NUMERICAL INVESTIGESTION OF DOUBLE GATE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR WITH SiO_2 GATE STRUCTURE

A thesis paper is submitted in Partial Fulfilment of the requirements for the award of Degree of Bachelor of Science in Electrical and Electronic Engineering.

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DECLARATION

The paper titled **"NUMERICAL INVESTIGATION OF DOUBLE GATE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR WITH SiO_2 GATE STRUCTURE"** is hereby acknowledged as the original work conducted at the laboratories of the Department of Electrical and Electronic Engineering, Daffodil International University. This paper fulfills a partial requirement for the degree of Bachelor of Science in Electrical and Electronic Engineering. I affirm that the content has not been previously submitted for any other academic qualification. Ethical and safety considerations have been diligently addressed, and all necessary approvals have been obtained. Participant rights and obligations have been duly recognized.

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Dedicated

To

Our Parents

For their endless love, support & Encouragement.

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LIST OF ABBREVIATIONS

FET	Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
DGMOSFET	Double Gate Metal Oxide Semiconductor Field Effect Transistor
TCAD	Technology Computer Aided Design
DIBL	Drain Induced Barrier Lowering
SCE	Short Channel Effect
Si	Silicon
SiO2	Silicon Dioxide
1D/2D/3D	1 Dimensional/2 Dimensional/3Dimensional

LIST OF SYMBOLS

Symbol	Name of Symbol
μ	Micro
∂	Partial
ε	Epsilon
Φ	Phi
∇	Del
ρ	Rho

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ABSTRACT

This thesis presents a numerical investigation of Double Gate Metal Oxide Field Effect Transistor (DGMOSFET) featuring a silicon dioxide (SiO_2) gate structure. As device scaling progresses, DG-MOSFETs have gained prominence due to their enhanced electrostatic control and reduced leakage currents compared to single-gate MOSFETs. Using advanced numerical simulations, we analyze key performance metrics, including threshold voltage, subthreshold slope, Drain Induced Barrier Lowering (DIBL), and on-off current ratio. The study examines the impact of gate oxide thickness, channel length, and doping concentrations on device performance.

Our findings reveal that the SiO_2 gate structure in DG-MOSFETs significantly mitigates short-channel effects and leakage currents while improving subthreshold slope and threshold voltage stability. The results underscore the importance of optimizing device dimensions and material properties to achieve superior electrical characteristics. This research provides valuable insights into the development of high-performance nanoscale semiconductor devices.

Keywords: Double Gate MOSFET (DGMOSFET), Silicon Di-oxide (SiO_2), Drain Induced Barrier Lowering (DIBL), Threshold Voltage, On-Off Current Ratio.

Chapter 1

INTRODUCTION

1.1 MOSFET

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a pivotal element for modifying or switching electronic signals. Although it's generally conceded as enjoying three outstations- drain(D), source(S), and gate(G)- it in fact encompasses a fourth terminal appertained to as the body(B). This outstation is generally connected with the source terminal, effectively rendering it a 3-terminal device, akin to other field- effect transistors. Despite the internal short- circuiting of both outstations, the physical device manifests only three outstations. The MOSFET has largely superseded the bipolar junction transistor in both analog and digital circuits.[1]

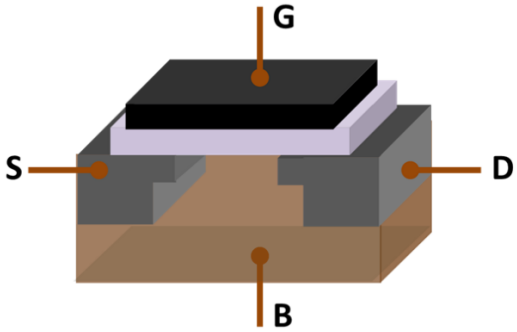

Fig1.1.1: MOSFET view with it’s four terminals Drain(D), Body(B), Source(S) & Gate(G).

The illustration labeled as Figure1.1.1 depicts a MOSFET with four outstations gate(G), body(B), source(S), and drain(D). An separating subcaste(depicted in white) serves to separate the gate from the body. In the improvement mode, a conductive channel is formed between the drain and source connections through the field effect caused by the voltage drop across the oxide. The improvement mode entails an increase in conductivity as the oxide field strength grows. This addition always results in the preface of carriers to the channel, also appertained to as the inversion subcaste. This channel may correspond of either electrons, known as an n-MOSFET or n-MOS, or holes, known as a p-MOSFET or p-MOS. specially, similar MOSFETs always parade the contrary substrate type, whereby a p- MOS is created using an n- type substrate and an n- MOS with a p- type substrate. [2]

1.2 Limitations of MOSFET

The usual MOSFET exhibits a restriction wherein the subthreshold swing remains fixed when IDS- VGS is intrigued on a log-lin scale. Accordingly, scoring a lower threshold voltage involves manipulating the IDS- VGS characteristics, sophisticating the optimization process for ultimate unlooked-for transition turn- on with gate voltage. specially, a 60mV measure in the threshold voltage VT results in a one- decade boost in the unacceptable current, which directly impacts stationary authority. Addressing these expostulations requires careful reflection and ingenious results within the field.

Figure1.2.1 depicts a true IDS- VGS symptomatic for a generally optimized usual MOSFET strutting a sub-threshold swing constrained to 60 mV/ decade at space temperature. A reduction in VT by relocating the symptomatic to the left necessitates taking an boost in leakage current. The logical wind data represents an optimized asymmetrical double-gate usual MOSFET from [2], which has been also shifted three moments. Such a measure may be achieved through manipulation of the gate work function, for illustration.

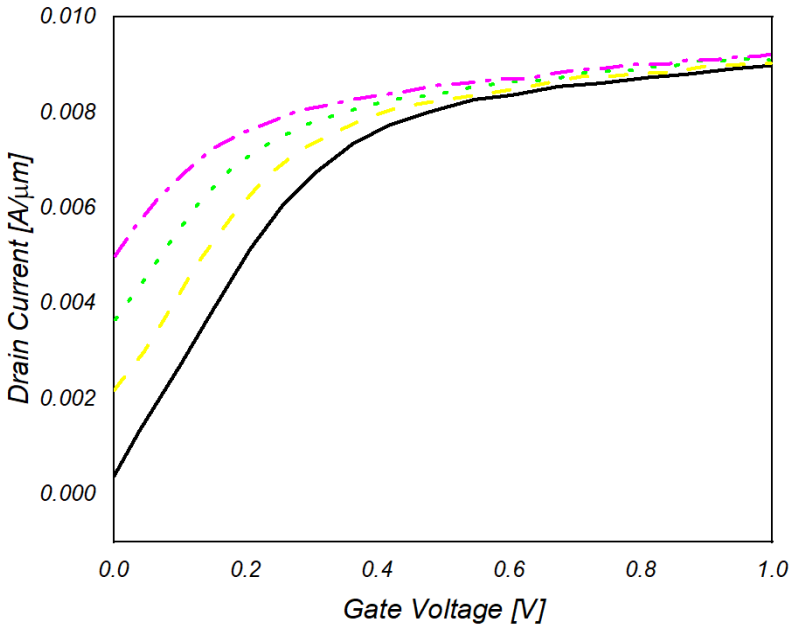

Fig1.2.1: A true IDS-VGS curve for highly-optimized usual MOSFET

1.3 Scaling

It's fascinating to observe the pivotal part of the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) in integrated circuits (ICs), especially due to their scalability capability. Over time, sweats have been made to minimize the size of nearly every semiconductor device in line with technological advancements. The MOSFET, which formerly featured channel lengths of several micrometers, has now been gauged down to nanometers in ultramodern intertwined circuits. According to Moore's law, the confines of the MOS transistor have been constantly dwindling since 1960 by a factor of 30. This continual reduction in size has brought about colorful advantages, including bettered circuit speed and effectiveness. Some of the positive impacts of dwindling MOS device confines include:

- Reduction in the length of the gate (LG) enhances the operational frequency of the circuit, resulting in faster performance.
- Smaller chip sizes lead to improved transistor efficiency and reduced cost of ICs.
- The consistent decrease in power consumption enables lower power usage for individual functions or a greater number of circuits operating within the same power constraints.

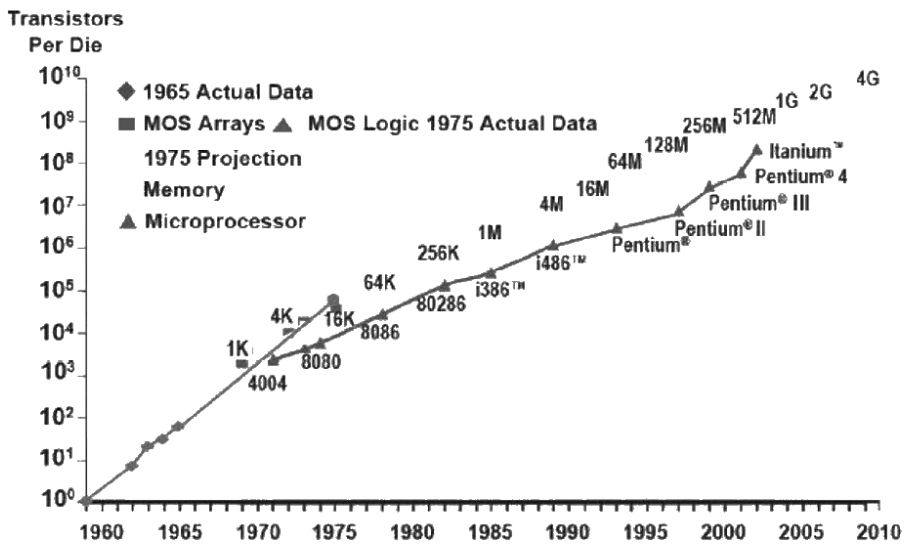

Fig 1.3.1: Moore’s law of scaling. [3]

Figure 1.3.1 illustrates Moore's law of scaling, demonstrating the consistent increase in transistor count on a single chip over time. CMOS technology offers an initial advantage through defined scaling laws. The International Technology Roadmap for Semiconductors

(ITRS) has established guidelines for spanning with reference to cost and authority consumption.

The ITRS 2010 (Figure1.3.2) indicates that by 2013, the 22nm technology node should have a physical channel proportion of 10nm or lower. This acquirement is attributable to the global collaboration of device masterminds, who have made controlled scaling, a process involving the modification of device boundaries, allowing a reduction in chip area without compromising long- channel interpretation, a reality, Dr. Dennard and his associates proffered this scaling path in 1972.

In addition to the reduction in device confines, spanning contributes to dropped dynamic power through voltage reduction. It's pivotal for both the perpendicular and side aspects of the transistor to gauge by the same factor to help short- channel goods and insure effective electrostatic control during lower bias fabrication. also, adding substrate doping attention by the same scaling factor can reduce the applied voltage.

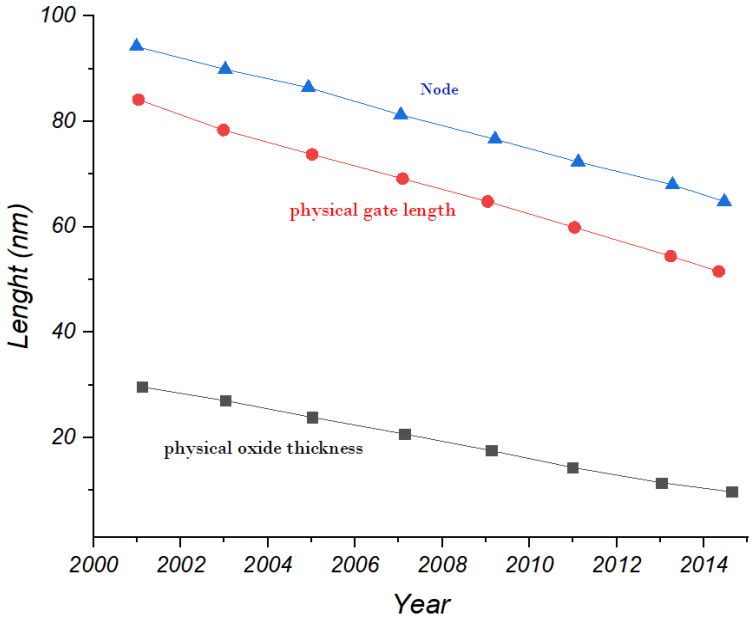

Fig1.3.2: gate length of scaling years (Courtesy: ITRS 2010)

It's intriguing to note the principles of scaling in MOSFET as described by Dennard. in 1974. According to Dennard's rules, all aspects of the device, including the threshold voltages, are gauged down by the same factor. Over time, it has been constantly observed that scaling, which involves reducing the physical confines of the transistor structure, has led to bettered bias performance and increased speed. One of the crucial aspects of scaling involves reducing the

gate length (LG) and the effective oxide consistence to increase the Cox and eventually enhance the ION. This increase in ION contributes to advanced circuit pets, reduced power consumption, and lower circuit area. Importantly, the power effectiveness of the circuit remains unchanged despite these variations.

The reduction in the dimensions of MOSFETs presents challenges in the fabrication process of semiconductor devices, requiring operation at significantly lower voltages and resulting in diminished electrical performance, thus necessitating circuit redesign. Additionally, the scaling of MOSFETs gives rise to various short-channel effects, including drain-induced barrier lowering (DIBL), punch-through, high leakage currents, and impact ionization, all of which contribute to the degradation of circuit performance. These short-channel effects persist despite efforts to optimize device parameters, ultimately diminishing the control of the channel through the gate and increasing leakage current, thereby adversely affecting the characteristics of the MOSFET.

With the rapid advancement of technology, the eventual limit to the reduction in size is increasingly difficult to ascertain. This downsizing holds the promise of creating superior equipment to prevent leakage. However, it is imperative to address the need for a solution for MOSFET in order to sustain the current trajectory of performance enhancement.

It's noteworthy that, as per R. Dennard scaling, the scaling of a MOSFET without altering the electric fields within the device can be achieved by reducing the device confines by a factor of 1/ κ, while adding the doping of the drain and source regions by a factor of κ. likewise, the voltage applied should be gauged by a factor of 1/ κ. This set of principles has been stuck to by experimenters since 1974, until more lately.

Dennard ‟ s scaling rules can no longer be followed as ahead. The figure1.3.3 shows the trend of scaling from the1.4 μm knot to the 65 nm knot. It can be seen that still there has been a drop in the force voltage VDD by about 20 of its original value, the reduction in the threshold voltage VT is much lower. This has happed only due to Dennard scaling. This had come in some other ways, like changing the doping of the channel region under the gate. On following the rules of gauging properly, there is no change in the electric fields inside a MOSFET. Hence there is no change in the threshold voltage also, unless we make some other changes.

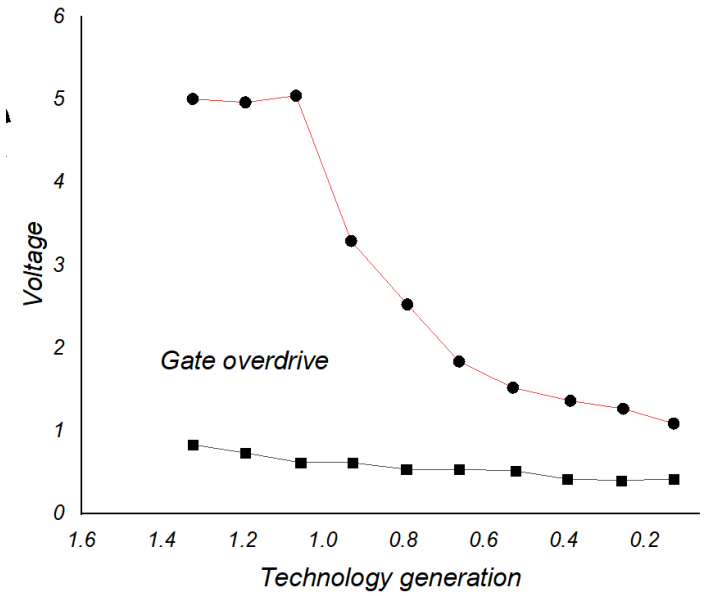

Fig1.3.3: The trend of threshold voltage and supply voltage scaling vs technology generation. V_{DD} decrease with device dimensions, but VT does not. [4]

Later much disquisition, it has been seen that to attack the problems faced by the conventional MOSFET, it's better to replace the device with some new bias rather of chancing results in the circuit design of the same. And swish way to break the problems would be to design a conventional MOSFET which will have a subthreshold swing of lower than 60mV/ decade at room temperature.

Multitudinous new ideas have been studied to reduce subthreshold swing to lower than 60mV/ decade at room temperature. Also two analogous bias will be explained which have been experimentally indicated. They are IMOS and MEMS NEMS switches.

1.4.1 IMOS

Figure1.4.1(a) shows IMOS. Which is a restarted p- i- n junction main purpose is to move into avalanche breakdown. Hence when the device is on its gate is neutralize from one of the junctions which leads to the conformation of a truly high electric field inthenon-gated portion of the i- region. [5]

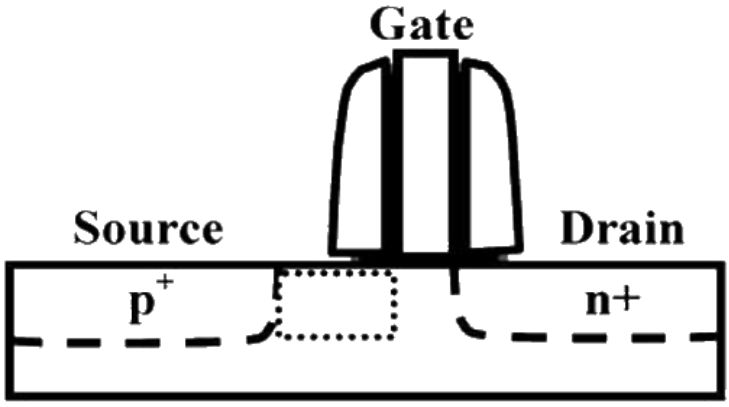

Fig1.4.1 (a): A typical IMOS structure in which a p-i-n diode is partially gated, with part of the intrinsic region left uncovered.

It has been seen from the experimental transfer characteristics of IMOS (impact ionization process) that it can truly small subthreshold swing along with high on- current [7]. From the following figure1.4.1 (b) which shows the transfer characteristics of IMOS, it can be studied that, its subthreshold swing is about 4mv/ decade for n- channel bias and about 9mV/ decade for p channel bias.

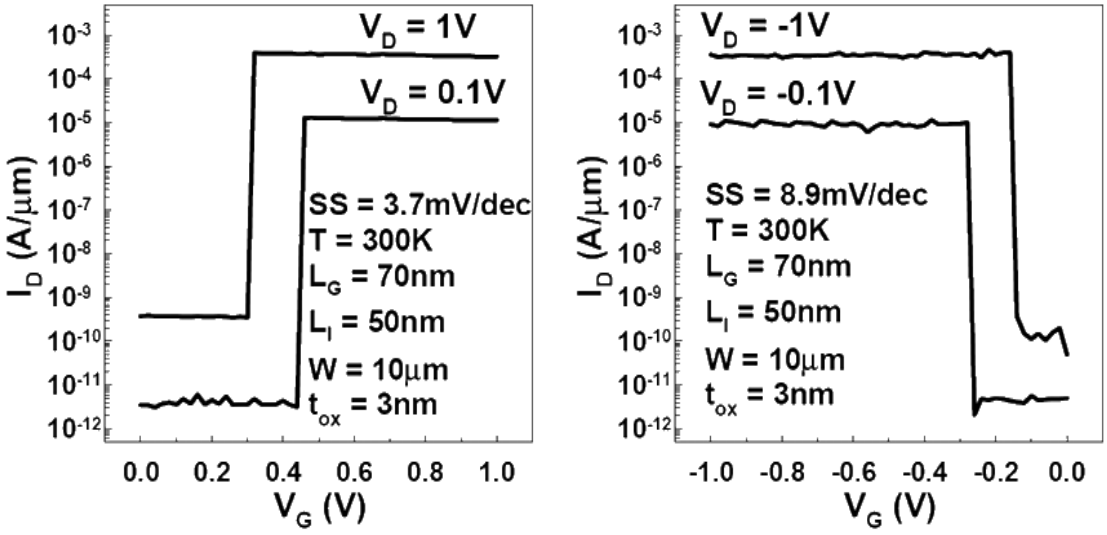

Fig 1.4.1(b) Measured IMOS IDS-VGS characteristics for n-channel (left) and p-channel (right) devise, from [6], where the source was biased at -5.5V.

The main problems with IMOS include scalability since there must always be a restarted and an ungated region between the source and drain, hot carrier declination since impact ionization inevitably creates hot carriers and these can go into the gate oxide, and the difficulty of low voltage operation, since high voltages are demanded in order to induce breakdown. Though IMOS gives lower subthreshold swing, there are multitudinous problems faced by it. As it requires both restarted and ungated regions of natural between the source and the drain for its conformation, it faces the problem of scalability. Another problem of IMOS is that of hot carrier declination. Hot carriers, which are created due to impact ionization can always go into the gate oxide. The coming problem is regarding its operation. It requires high voltage for its operation so as to induce breakdown.

1.4.2 MEMS/NEMS

The coming small swing switch is the electro-mechanical relay which can be also on the NEMS i.e. nanometer scale or on the MEMS i.e. micron scale. NEMS switches can be divided into either two-terminal bias or three-terminal bias. Though the two-terminal bias may have truly low swing values [8], they warrant in terms of circuit operations. Hence the conventional MOSFETs can be replaced by the three-terminal bias. This type of switch can have multitudinous possible designs. Two of the designs are explained below.

One of the design involves the fabrication of a flexible stake shaft which is electrically connected to source terminal(figure1.4.2(a)). This shaft is actuated by a gate electrode which is present under and also it's being down so that it touches the drain electrode during the on-state. The coming design uses a typical MOSFET layout, with drain, channel, and source, as in the two bias shown in Figure.2.11

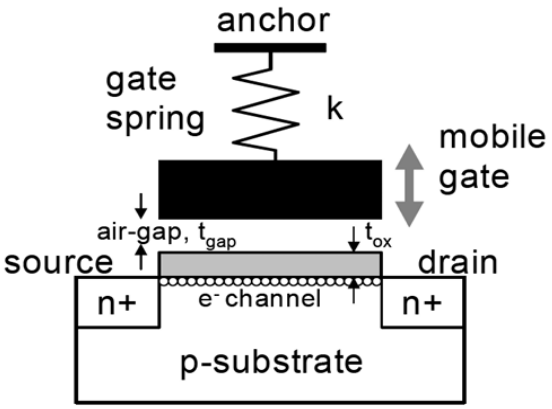

Fig1.4.2.1(a)

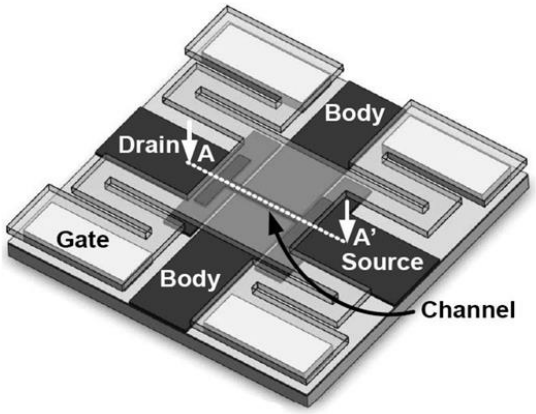

Fig1.4.2.1(b)

Fig1.4.2.1: Two possible designs for MOSFET like MEMS relays with a source, drain, and gate [9].

Another possibility is to use a more typical MOSFET layout, with source, channel, and drain, as in the two bias shown inFig.1.4.2.1. The first design(Figure1.4.2.1(a)), has a gap filled with air in between the gate contact and the gate dielectric. The gate of this design moves up and down during off- state and on- state singly.

The alternate(Figure1.4.2.1(b)) consists of the drain and source regions on the substrate. This design consists of a gate/ channel that can be moved i.e. it can be pulled down into contact with the drain and source when it's in the on- state.

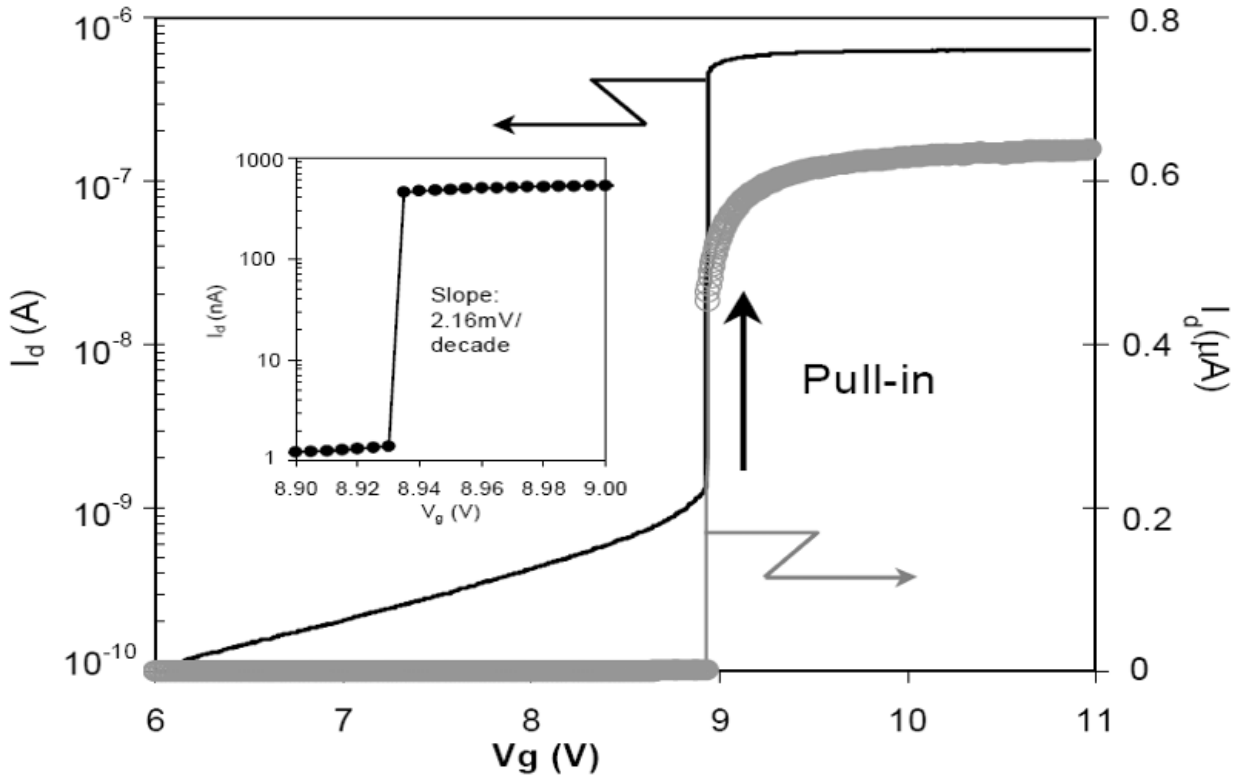

Fig: 1.4.2.2(a)

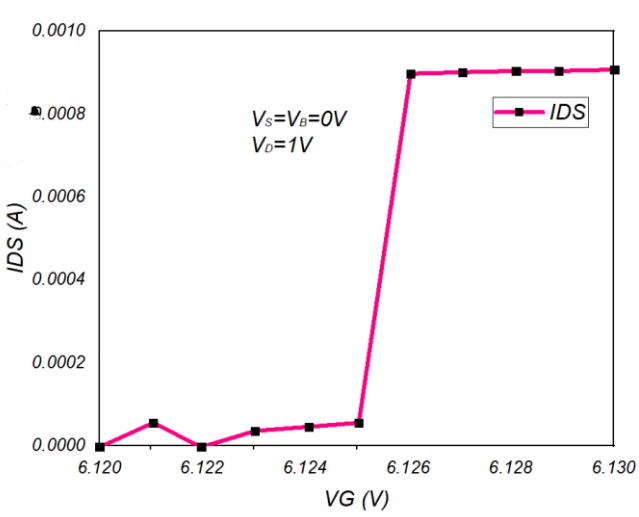

Fig: 1.4.2.2(b)

Fig1.4.2.2: Measured IDS-VGS characteristics for the MEMS switches demonstrating extremely small subthreshold swings .

The swing in this type of device is set by the voltage step size, has no abecedarian limit, and can approach zero. (a) Junction leakage is still present for this relay design (b) Off- state current is much lower for a design in which the source and/ or drain is physically separated from the MOSFET channel. [9,10]

These switches can be used in place of the conventional MOSFET because of their benefits like veritably low off currents along with high ON currents, and small subthreshold swings. But they also face a many disadvantages like lower speed and due to their mechanical nature, they also have to face the problem of trustability, like the structural damage caused when the two pieces need to touch each other and also come back piecemeal millions of times.

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1.5 Objectives

The following are the main goals of this thesis:

The primary objective of double gate MOSFETs is to enhance transistor performance and scalability in advanced integrated circuits, particularly as device dimensions shrink to nanometer scales. We also tried to improve performance by reducing channel doping such as:

- Enhanced Electrostatic Control
- Reduction of Short Channel Effects (SCE)
- Lower Leakage Currents
- Improved switching behavior

Which are significant challenges in traditional single-gate MOSFETs. Double gate MOSFETs also aim to increase drive current and reduce power consumption, enabling the continued advancement of high-performance, low-power electronic devices.

1.6 Motivation

We introduced a double gate structure in this paper to enhance MOSFET performance. Using TCAD simulation, we suggested and evaluated a silicon hetero structure based double gate MOSFET. The motivation for using Silvaco TCAD in designing double gate MOSFETs lies in the critical need to enhance device performance and scalability as technology advances towards smaller nanometer nodes. Double-gate MOSFETs provide improved electrostatic control, significantly reducing short channel effects and enhancing key performance metrics such as drive current and leakage current. Silvaco TCAD offers an advanced simulation platform that

enables precise modeling and optimization, facilitating cost-effective virtual prototyping and deeper insights into complex physical phenomena [2]. Silvaco TCAD provides a comprehensive simulation environment that allows for precise modeling and optimization of these devices, enabling cost-effective and efficient virtual prototyping. By leveraging advanced physical models and customization options, Silvaco TCAD helps in understanding complex phenomena and ensuring the scalability of double-gate MOSFETs for next generation semiconductor technologies.

1.7 Thesis Organization

After the introduction, these are the following chapters which are included in this thesis:

Chapter 2: This chapter is about the works done by the researchers related to this topic in the past.

Chapter 3: This chapter discusses devices simulation tools, which are software or analytical tools used to extract the device behavior.

Chapter 4: This chapter discusses about the project management task, schedule & milestones.

Chapter 5: this chapter discusses about the materials used in the simulation of the proposed double gate MOSFET.

Chapter 6: This chapter discusses the structure and fabrication of the DGMOSFET. We bandy how the DGMOSFET was designed in Silvaco Atlas. We depict 2D and 3D numbers of the device itself and list out the parameters of each material.

Chapter 7: This chapter examines the simulation affair's characteristics and provides a theoretical explanation. This chapter also included the confirmation of the affair electrical characteristics.

Chapter 8: This chapter contains the work's overall conclusion. The discovered enhancement is stressed. This chapter also discusses unborn work.

Chapter 2

LITERATURE REVIEW

2.1 INTRODUCTION

The Double-Gate MOSFET (DG MOSFET) has emerged as a significant advancement in semiconductor technology, effectively addressing the scaling challenges encountered by traditional single-gate MOSFETs. As device dimensions continue to decrease to the nanometer scale, conventional MOSFETs face notable issues such as short-channel effects, leakage currents, and reduced drive current capabilities, which significantly impede the performance and reliability of transistors in ultra-scaled integrated circuits. The advanced structural design of the DG MOSFET offers a robust solution to these challenges, positioning it as a focal point of contemporary nanoelectronics research and development. The DG MOSFET is characterized by the presence of two gates that concurrently regulate the conductive channel from opposing sides. This configuration provides superior electrostatic control over the channel, effectively suppressing shortchannel effects and enhancing overall device performance. The dual-gate structure enables more efficient modulation of the channel charge, resulting in a steeper subthreshold slope, higher drive currents, and reduced leakage currents. These improvements are particularly advantageous for low-power and high-speed applications where energy efficiency and switching speed are paramount. Scalability is a fundamental advantage of DG MOSFETs. As transistor dimensions continue to diminish, maintaining control over the channel becomes increasingly challenging with single-gate MOSFETs. The enhanced ability of DG MOSFETs to regulate channel electrostatics makes them better suited for future technology nodes, ensuring sustained advancements in semiconductor performance in accordance with Moore's Law. Furthermore, the DG MOSFET structure facilitates innovative device architectures, such as FinFETs and Trigate transistors, which are already being implemented in advanced technology nodes by leading semiconductor manufacturers. Despite these advantages, the fabrication of DG MOSFETs presents certain challenges. The precise alignment of the two gates and the requirement for high-quality dielectric materials are critical for optimal performance. Achieving the necessary precision necessitates advanced lithography and deposition techniques, which can elevate production complexity and costs. Nonetheless, ongoing research and development endeavors are dedicated to surmounting these challenges and enhancing the manufacturability of DG MOSFETs. In summary, DG MOSFETs represent a significant progression in transistor technology, offering solutions to the scaling

issues faced by conventional MOSFETs. Their superior control over short-channel effects, enhanced drive currents, and scalability position them as promising candidates for future high-performance, low power electronic devices. As research advances, DG MOSFETs are anticipated to play a pivotal role in the ongoing evolution of semiconductor technology. [11]

2.2 I-V Characteristics of DG MOSFET

The current-voltage (I-V) characteristics of double gate MOSFETs (DGMOSFET) demonstrate their superior performance compared to traditional single-gate MOSFETs, owing to enhanced electrostatic control. The transfer characteristics (I_D-V_{GS}) of DGMOSFET exhibit a steeper subthreshold slope and higher drive currents, attributed to the dual-gate structure enabling improved channel control and reduced leakage currents. As a result, a lower subthreshold swing, typically around 60 mV/decade, indicates more efficient switching. The output characteristics (I_D-V_{DS}) portray enhanced output conductance and higher output resistance, as the dual gates effectively mitigate short channel effects and drain induced barrier lowering (DIBL). Consequently, DGMOSFET sustain stable current levels at higher V_{DS} values, crucial for analog and high-frequency applications. The dual-gate configuration ensures symmetric electric field distribution and precise modulation of the channel potential, leading to higher on-currents (I_{ON}) and lower off-currents (I_{OFF}), thereby enhancing both performance and energy efficiency. The improved channel control reduces variability and sensitivity to short-channel effects, rendering DGMOSFET highly suitable for scaling down to nanometer dimensions. These characteristics underscore the potential of DGMOSFET in delivering high-performance, low-power electronic devices, reinforcing their significance in the future of semiconductor technology. [12]

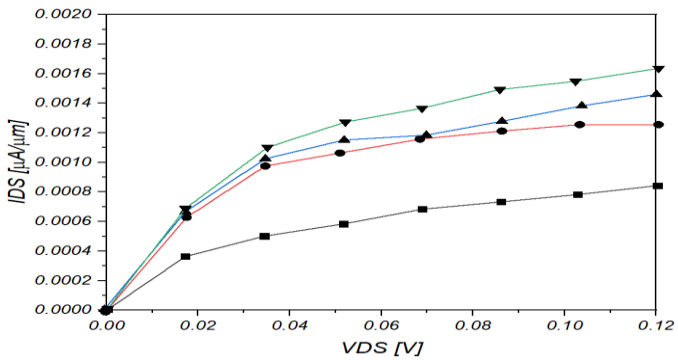


Fig2.2.1: I-V characteristics of DGMOSFET.

2.3 Compare and Contrast

When compared to other types of FETs, Double Gate MOSFET (DG MOSFET) has some advantages and disadvantages. Then are some exemplifications.

2.3.1 Double Gate MOSFET vs Single Gate MOSFET

- **Merit of DGMOSFETS:** In the off state, the DG MOSFET experiences a much lower leakage current compared to the SG MOSFET. This is crucial for battery life in portable devices and overall power efficiency in circuits.
- **Merit of SGMOSFETs:** DG MOSFETs require a more complex fabrication process compared to SG MOSFETs. The double gate structure necessitates precise control over gate placement and channel formation, adding steps and potential challenges to production.

2.3.2 DGMOSFETs vs. FinFETs

- **Merit of DGMOSFETS:** For a given level of performance, DG MOSFETs can potentially achieve a smaller footprint compared to FinFETs. This is because DG MOSFETs utilize a planar structure, allowing for denser packing of transistors on an integrated circuit.
- **Merit of FinFETs:** The 3D fin structure of FinFETs provides better electrostatic control over the channel, leading to more effective suppression of short-channel effects. This becomes crucial for achieving high performance in very small transistor sizes.

2.3.3 DGMOSFETs vs. TFETs

Merit of DGMOSFETS: DG MOSFETs operate based on the principle of field-effect modulation, where the gate voltage controls the formation of a conducting channel. This allows for a more efficient flow of current when the transistor is turned on.

Merit of TFETs: Due to the tunneling mechanism, TFETs can achieve significantly lower leakage currents, making them attractive for ultra-low power applications.

2.4 Why DG MOSFET better than the other FET

Double Gate (DG) MOSFETs present a compelling array of advantages over alternative FETs. They feature a steeper subthreshold slope in the I-V curve, resulting in more distinct on-off transitions and reduced leakage current in comparison to SingleGate MOSFETs. This attribute contributes to enhanced switching speeds and augmented power efficiency. While FinFETs offer superior control over short-channel effects, DGMOSFETs have the potential to achieve a smaller footprint for comparable performance due to their planar structure. Furthermore, DGMOSFETs offer a more favorable equilibrium between driving current and power consumption when juxtaposed with Tunnel FETs, rendering them better suited for general-purpose applications necessitating high performance without substantial compromise on power efficiency. Notwithstanding, the intricate fabrication process of DGMOSFETs renders them more expensive than simpler FET options. Consequently, the optimal FET choice hinges on the specific requirements of the application, with DGMOSFETs excelling in delivering a harmonious blend of performance, power efficiency, and area efficiency.

2.5 Summary

The chapter offers a comprehensive overview of Double Gate MOSFETs (DGMOSFETs), a promising technology for future Nano electronic devices. It begins with an exploration of the current voltage (I-V) characteristics of DGMOSFETs, detailing how the dual gate configuration influences current flow and device operation. Subsequently, a comparative analysis between DGMOSFETs and conventional MOSFETs is presented, highlighting key differences in parameters such as subthreshold slope, leakage current, and scalability. The chapter then discusses the advantages of DGMOSFETs over other FET technologies, emphasizing how the double-gate structure provides superior control over the channel, resulting in improved performance metrics such as lower power consumption and better electrostatic integrity. In conclusion, the chapter asserts DGMOSFETs as a compelling technology for future advancements in miniaturization and low-power electronics.

Chapter-3

DOUBLE GATE MOSFET SIMULATION TOOLS & SOLUTION TECHNIQUE

3.1 Introduction

There are colorful device simulation tools available to simplify analysis. Then in our exploration work on double-gate MOSFET. We've used Silvaco atlas Tcad for device simulation and chancing some characteristics. The OriginLab has also been used for fresh wind birth, analysis, and confirmation.

3.2 Silvaco TCAD

3.2.1 Introduction to Silvaco ATLAS

ATLAS is a two and three- dimensional semiconductor device simulator that is physically predicated. It predicts or calculates the electrical geste of specified semiconductor structures and provides information about the internal physical parcels of the device. ATLAS can be used as a standalone tool for standard device simulation or as a core tool in the SILVACO VIRTUAL WAFER FAB simulation terrain. Device simulation fits between process simulation and SPICE model birth in the sequence of calculating the impact of process variables on circuit performance. ATLAS is a medicines- predicated device simulator developed by SilvacoInc. in the United States. It was originally designed for silicon- predicated MOS transistor modeling but has agone been expanded with multitudinous modular extensions, making it suitable for modeling organic displays, photovoltaic cells, and multitudinous other bias. With this tool, the electrical geste of a semiconductor device can be predicted, as can the physical process associated with device operation. The device structure will be approached as a two or three- dimensional grid with several grid points, also known as bumps. A set of partial demarcation equations derived from Maxwell's laws and applied to these grids can be used to pretend carrier transport in the device. This system can be used to calculate performance under DC bias, AC voltage, or flash conditions. This system can be used to calculate performance under DC bias, AC voltage, or flash conditions. medicines- predicated simulations are more logical in the sense that they combine theoretical vatic nation with complementary knowledge. Hence it provides different results when compared to empirical which gives better

approximations with the being data and offers accessible interpolation. medicines- predicated simulators are less precious and hastily, and they can predict quantities that are impossible to measure. The main disadvantage is the demanded knowledge of device medicines and the incorporation of time consuming numerica1 procedures to break the equations. In Atlas, the device simulation process must be specified by defining the physical structure of the device to be dissembled and concluding the applicable modelequation.However, it can be created and included using the tool's C- guru function, If the model equation is not formerly in the library. This makes it more useful.

3.2.2 ATLAS Inputs and Outputs

The diagram in Figure 3.1 illustrates the various data flows into and out of the ATLAS system. The advanced ATLAS simulations utilize two primary input lines known as command and structure lines. The command line consists of ATLAS commands and syntax, while the structure line involves a file that represents the simulated structure. Additionally, ATLAS incorporates three distinct types of output files. The first type is the run time output file, which provides detailed information on the simulation's progress, error messages, and warning notifications. The log file is another kind of output file that records all terminal voltages and currents from the device simulation. The third type is the result file, which stores 2D and 3D data related to the values of result variables within the device at a specified bias point.

DeckBuild

The DeckBuild Command window, penetrated through the Commands button on DECKBUILD’s main screen, serves as a precious tool for specifying input lines. When initiating a simulation, it's imperative to outline the device structure type and result process within DeckBuild. This point-rich tool provides an intertwined platform for managing, creating, and running semiconductor simulation systems and designs. It encompasses a script editor for casting simulation scripts, tools for imaging and assaying results, and intuitive controls for overseeing multiple simulations. DeckBuild employs a specialized command language for precise simulation control and seamlessly integrates with other Silvaco tools, including ATLAS.

TonyPlot

TonyPlot offers visualization and graphic features analogous to visage, drone, views, labels, and the capability to support multiple plots using data saved in an ATLAS log train. It also provides a range of TCAD-specific visualization functions, including plate emulation, 1D cut lines from 2D structures, labeling for displaying vector flux, integration of log or 1D data lines, as well as completely customizable TCAD-specific colors and styles. also, TonyPlot supports the display of 1D, 2D, and 3D plots, enabling druggies to effectively interpret data from semiconductor processes and device simulations. By exercising TonyPlot, druggies can induce figure maps, cross-sectional views, and dynamic graphs to dissect electrical, thermal, and structural aspects of bias, thereby easing a deeper appreciation and optimization of semiconductor technologies on a global scale.

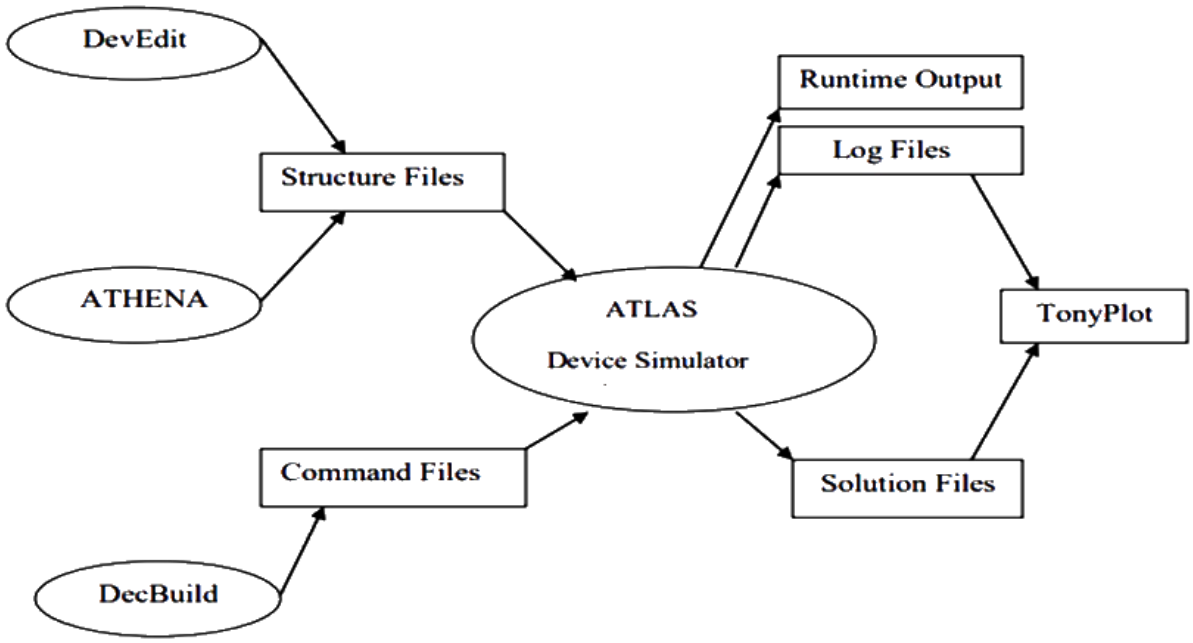


Fig. 3.2.1 Circuit diagram of ATLAS Input and Output

3.3 Technology computer-aided design (TCAD) model

TCAD(Technology Computer-Backed Design) is a simulation software tool used to model and pretend the physical geste of semiconductor bias. These models are embedded in physical principles and can directly prognosticate the electrical, thermal, and optic geste of bias. Extensively employed in semiconductor assiduity, TCAD models are necessary in the design,

optimization, and characterization of colorful semiconductor bias, including GAAFETs(Gate All Around Field- Effect Transistors). Employing numerical styles, TCAD models break partial discriminational equations that describe the device's physical gesture. For case, Poisson's equation describes the device's electrostatics, while the drift- prolixity equations explain carrier transport within the device. These equations are answered using numerical ways similar as finite element styles, finite difference styles, or Monte Carlo simulation. TCAD models can pretend colorful device characteristics, including current- voltage and capacitance-voltage characteristics, as well as temperature biographies. likewise, they can optimize device performance by reducing leakage current or enhancing device speed. also, TCAD models can pretend device fabrication processes similar as ion implantation and drawing to prognosticate the impact of process variations on device performance. These models are precious tools for semiconductor device design and optimization, as they contribute to reducing design cycle time and costs. They're considerably employed by semiconductor companies and exploration associations to pretend and optimize the performance of colorful semiconductor bias, including DG MOSFETs.

3.4 Equations used in Simulation

3.4.1 The Newton equation

The movement of electrons in the device is described by the Newton equation, generally appertained to as the durability equation It connects the drift haste and carrier attention to the current viscosity. The DG MOSFET's Newton equation looks like this:

$$\partial J/\partial x = qn\mu E + qDn(\partial n/\partial x)$$

The variables J, q, n, and E represent the current density, electronic charge, electron concentration, electron mobility, electric field, and electron diffusion coefficient, respectively.

3.4.2 poisson’s equation

To simulate the electrostatics of the GAAFET device, use Poisson's equation. It explains the connection between the device's charge density and electric potential. Information on the possible profile inside the device can be obtained by solving Poisson's equation.

$$\nabla \cdot (\varepsilon \nabla \Phi) = -\rho$$

Where ρ is the charge density, Π is the electrostatic potential, and ε is the material's dielectric constant.

3.5 Summary

The preceding chapter has provided a comprehensive understanding of the simulation of Double Gate (DG) MOSFETs using Silvaco ATLAS, a widely utilized technology computer-aided design (TCAD) software. It has introduced the core functionalities of ATLAS, elucidating its pivotal role in device simulation. The chapter has delved into the diverse input parameters essential for defining a DGMOSFET in ATLAS, and has elucidated the resultant outputs that yield valuable insights into device performance. Furthermore, it has expounded upon DeckBuild, an instrumental tool for automating script generation and streamlining the simulation process. Additionally, the chapter has introduced TonyPlot, a software designed for the visualization and analysis of simulation data. Lastly, it has provided an explanation of the TCAD models utilized by ATLAS, while also exploring the fundamental equations governing the simulation of DGMOSFET behavior. This knowledge equips individuals with the proficiency to effectively utilize simulation tools for the purpose of design exploration and optimization of DGMOSFET device.

Chapter 4

PROJECT MANAGEMENT

4.1 Task, Schedule and Milestones

4.1.1 Task

The primary objective of this project is to design and analyze a Double Gate Metal Oxide Semiconductor Field Effect Transistor (DGMOSFET) using Silvaco TCAD software. The materials used include silicon for the semiconductor, silicon dioxide for the gate dielectric, and aluminum for the gate conductor. [13] First of all Comprehensive review of being exploration on DGMOSFETs to understand design principles and performance criteria & how to design it & pretend it in Silvaco software. Also we Configuration of the Silvaco TCAD terrain, including material parcels and device figure. Generate the device structure there are some set up in Silvaco software these is simulator specification, mesh definition, region definition, electrode specification, doping specification, contact specification. Perpetration of the DGMOSFET design in Silvaco TCAD and running simulations to dissect electrical characteristics. Fine-tuning the design parameters to achieve optimal performance grounded on the simulation results. Assaying the simulation data to prize crucial performance criteria similar as threshold voltage, on/ off current rate, and subthreshold pitch.

4.1.2 Schedule

The design is planned over a period of 8- 10 weeks, conducting a literature review and gathering background information. Setting up the simulation terrain in Silvaco TCAD. Insure a functional DG- MOSFET structure is created in Athena with proper material delineations. Corroborate the simulation setup in Atlas is configured for our chosen accoutrements and transport models. Also design the original DG- MOSFET model and running primary simulations. Run simulations to reach gate voltage and dissect drain current characteristics. In the few weeks later we defined the prize crucial device parameters like threshold voltage, sub-threshold pitch, on-current, and out-current. Assaying the simulation data and rooting performance criteria. Then interpret the results in the environment of the literature review and identify implicit areas for optimization. Last week we decide finalizing on the analysis, upgrade

the DG- MOSFET design to achieve asked performance pretensions. Finishing the attestation and preparing the design report.

4.1.3 Milestones

Basically we are set some milestone in our project. A thorough understanding of DGMOSFET design principles and performance criteria. In week 4 we're successfully configure of the Silvaco TCAD terrain with all necessary accoutrements and parameters. Completion of the original device design and primary simulation runs. Achieving an optimized design with bettered performance characteristics. Detailed analysis of simulation results and performance evaluation. Submission of the comprehensive design report establishing all findings and results. Understanding the trade- offs between different design choices is essential for achieving optimal DGMOSFET performance. This section describes the start and finish of a project, and mark the completion of a major phase of task. Justification can be made on how the schedule/milestone is different from the mentioned one in introduction chapter.

4.2 Resources and Management

4.2.1 Resources

In this paper there are several types of sources & management system that we face and included Software Resources, Hardware Resources, and Human Resources etc. Essential software for simulating semiconductor devices as a resources the Key components include ATLAS for device simulation and Athena for process simulation. The suite provides comprehensive tools to model and analyze the Double Gate MOSFET. In Computing Infrastructure high-performance workstations or servers are required to run complex simulations efficiently. Specifications should include multicore processors, large memory capacity, and high-speed storage solutions. And for data reliable and secure storage systems for storing simulation data, results, and backup files. Cloud-based storage can also be considered for scalability and accessibility, and writing based storage can also be considered for accessible in software input data. Comprising semiconductor device engineers, simulation experts, and data analysts. Each member should have expertise in their respective fields and proficiency with Silvaco TCAD tools. All of members to coordinate tasks, manage timelines, and ensure that milestones are met. In the reference materials with conduct technical literature Access to scholarlyarticles, books, and previous research on DGMOSFETs, semiconductor physics, and TCAD simulations, Origin plot to plot graph, operation & modeling of the MOS Transistor etc. And

for documentation User manuals and technical support from Silvaco for troubleshooting and advanced simulation techniques. [14]

4.2.2 Management

As stated previously, MOSFET (metal oxide semiconductor field effect transistor) has gained a lot of attention in recent years due to its potential to overcome the limitations of conventional planar transistors. That's why we managed this project & continue to task & complete coherently. In the management of project planning, resource allocation, monitoring and control, risk management & communication with team coordination each time & completion the task. First we are dividing the project into smaller tasks such as literature review, simulation setup, design implementation, optimization, data analysis, paper review, software works, and documentation with discuss our supervisor. Then creating a timeline for each task with specific start and end dates to ensure systematic progress and timely completion. The resource allocation separate detailed budget planning for software licenses, hardware purchases, paper printing, and other miscellaneous expenses. Then we divide and assigning specific tasks to team members based on their expertise and experience. We are always monitoring and control regular meetings to review the progress of each task, address challenges, and make necessary adjustments to the schedule or resources and paper work. Implementing quality control measures to ensure the accuracy and reliability of simulation results. Sometimes we face risk identification like Identifying potential risks such as software issues, hardware failures, or data loss, mind loss, delete data, accurate data graph etc with collaborate our supervisor. Developing strategies to mitigate identified risks, such as regular data backups, maintenance of hardware, and access to technical support, mentally support of us, data get back, value of different dimension etc. In the main term of is good communication with us, Ensuring effective communication within the team through regular updates, meetings, and collaborative tools with a meeting or face to face. And periodic reporting to our supervisor on project status, milestones achieved, and any issues encountered in that time. [15]

4.3 Lesson Learned

In the part of lesson learned from this technical & hand work part we learn as Simulation Accuracy, Device Performance, Learning Curve, Resource Allocation, Management, Research and Development & Continuous learning & Communication. The field of semiconductor technology is rapidly evolving. Staying updated with the latest research and developments is necessary to incorporate cutting-edge techniques and materials into the project simulation.

Accurately lesson learning & defining the material properties of silicon, silicon dioxide, and aluminum is crucial. Ensuring the use of up-to-date and precise material data enhances the reliability of the outcomes. The quality of the simulation mesh directly affects the accuracy of the results. A well-optimized mesh can provide more accurate simulations without excessively increasing computational load. We learn also be through simulations, it was observed that the threshold voltage of the DGMOSFET is highly sensitive to the gate-oxide thickness and the work function of the gate material. The learning also the device performance is also affected by the channel dimensions. Scaling the device requires careful consideration of short-channel effects and maintaining an optimal aspect ratio.The software proficiency with learning curve. Gaining proficiency in using the various tools within the Silvaco tcad suite, such as ATLAS for device simulation and Athena ffor process simulation, requires a significant learning period.

Practical hands-on experience and referring to user manuals are essential for mastering these tools. Setting up simulations correctly involves understanding the thinness of each tool. This includes defining boundary conditions, applying appropriate physical models, and ensuring convergence criteria are met. To allocate for time management allocating sufficient time for each phase of the project, from literature review to final documentation, is critical. Underestimating the time required for complex simulations can lead to delays. Effective communication and coordination among team members, conduct with supervisor, including regular progress meetings and collaborative problem-solving, play a crucial role in the timely completion of the project. Keeping track of software licensing, hardware expenses, and personnel costs is essential. Documenting the entire process meticulously and sharing findings through reports or publications contributes to the broader research community and aids in future projects.

Chapter 5

MATERIAL SYSTEM AND PARAMETER

5.1 Introduction to material used

Based on the SiO2 heterostructure, we suggested a numerical investigation of Double Gate MOSFET (DGMOSFET) with SiO2 Gate Structure. We employed a single-layer SiO2 as a high-K dielectric layer in the gate stacking. Aluminum was our contact material. The primary components of the DGMOSFET are silicon and silicon dioxide, or SiO2.

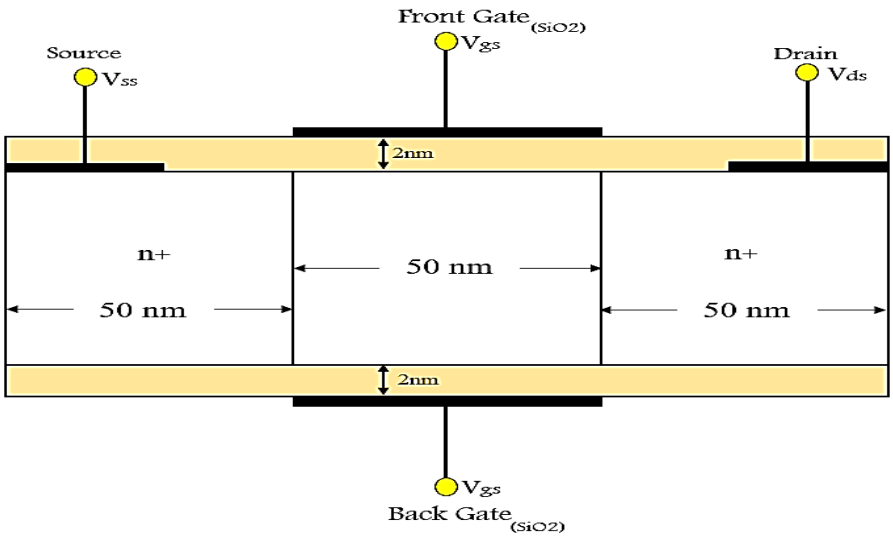


Fig5.1.1: Schematic representation of DGMOSFET

5.2 Silicon (Si)

Silicon (Si) is a material that has several properties that made it attractive for use in our DGMOSFET (Double Gate Metal Oxide Semiconductor Field-Effect Transistor) device. Silicon is considerably used in MOSFETs (Metal Oxide- Semiconductor Field- Effect Transistors) due to its combination of profitable parcels that are critical for semiconductor device performance. Silicon's electrical characteristics, including an ideal band-gap of 1.12 eV, allow for effective operation over a wide range of temperatures, icing the trust ability and effectiveness of the MOSFETs in colorful conditions. Its capability to form a high- quality native oxide, silicon dioxide (SiO_2), is pivotal for creating a stable separating subcaste for the MOS structure, which is essential for controlling the gate in MOSFETs. Likewise, silicon is abundantly available in the Earth's crust, making it a cost-effective choice for large- scale

product. The well- established silicon processing technology benefits from decades of assiduity refinement, performing in high manufacturing yields and reliable device performance. Also, silicon's balanced carrier mobility is essential for fast switching pets, and its mechanical strength supports device integrity during manufacturing and operation. Silicon offers several advantages in the fabrication of MOSFETs (Metal- Oxide- Semiconductor Field- Effect Transistors) that make it the material of choice in the semiconductor assiduity. The conformation of a high- quality native oxide, silicon dioxide (SiO_2), is critical for the gate sequestration in MOSFETs, furnishing excellent electrical sequestration and stability. Silicon's abundant vacuity and cost- effectiveness make it economically feasible for large- scale product. Also, the expansive structure and mature technology for silicon processing result in high manufacturing yields and device trust ability. Also, silicon's balanced carrier mobility supports presto switching pets, which is essential for the performance of ultramodern electronic bias. These advantages inclusively contribute to silicon's dominance in MOSFET technology, enabling advancements in electronics and integrated circuits [16].

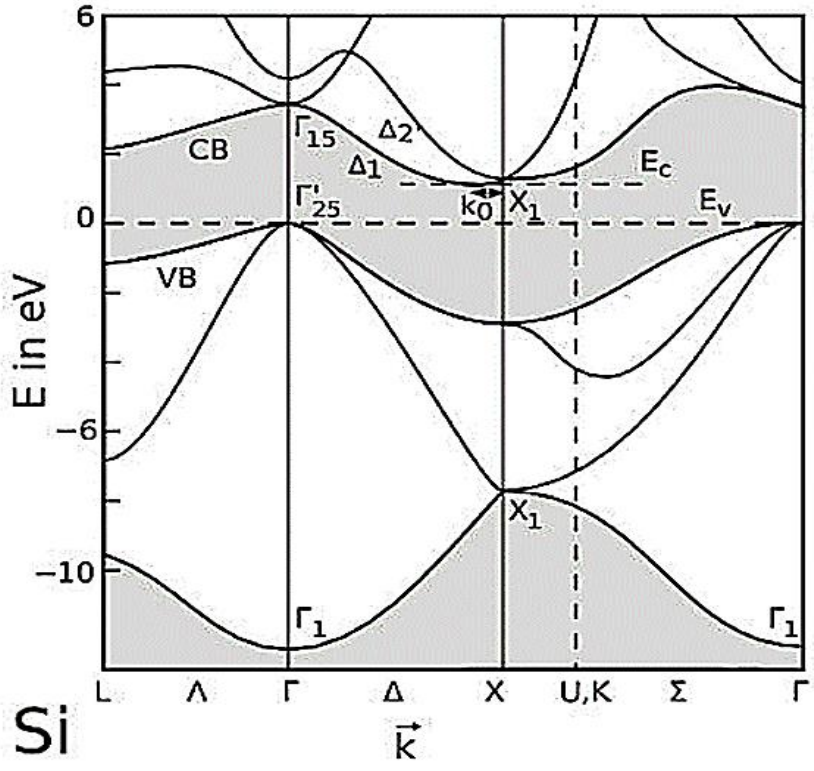


Fig5.2.1: Band Diagram of Silicon

5.3 Silicon Di-oxide (SiO2)

SiO2 (silicon di-oxide) is a popular material used in the gate di-electric layer of DGMOSFETs (Double Gate Metal Oxide Semiconductor Field Effect Transistors) for several reasons. The dielectric constant of silicon dioxide (SiO_2), also known as the relative permittivity, is approximately 3.9. This value indicates the material's ability to store electrical energy in an electric field relative to the vacuum. The dielectric constant of SiO_2 is a critical parameter in the design and performance of MOSFETs and other semiconductor devices, as it influences the capacitance of the gate oxide layer, thereby affecting the device's electrical characteristics and performance.

Silicon dioxide (SiO_2) is used as a gate dielectric material in MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) primarily because of its excellent separating parcels and comity with silicon. SiO_2 has a dielectric constant of roughly 3.9, which provides a good balance between capacitance and separating capability. This dielectric subcaste is pivotal for controlling the gate voltage and, latterly, the current inflow through the MOSFET. The high-quality native oxide that SiO_2 forms on silicon shells ensures a dependable and stable separating subcaste, which minimizes leakage currents and enhances device performance. Also, SiO_2 can be thermally grown on silicon substrates, creating a flawless and disfigurement-free interface that's essential for the effective operation of MOSFETs. The stability and robustness of SiO_2 under colorful operating conditions further contribute to the life and trust ability of semiconductor bias. These parcels make SiO_2 an ideal material for the gate dielectric in MOSFETs [16].

5.4 Aluminum (Al)

Aluminum is generally used as a captain material in MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) due to its excellent electrical conductivity, ease of fabrication, and comity with silicon processing technologies. Aluminum has a low resistivity (about 2.65 $\mu\Omega \cdot$ cm), which allows for effective current inflow and minimizes power losses in the inner connects and connections within the MOSFET. It can be fluently deposited using ways similar as sputtering and evaporation, which are well- integrated into standard semiconductor fabrication processes. Also, aluminum forms good electrical contact with silicon, especially when combined with applicablehedge essence to help issues similar as silicon prolixity. It’s fairly low melting point (660°C) makes it suitable for use in processes that don't bear high-temperature stability, simplifying manufacturing way and reducing costs. Also, aluminum's

capability to form a native oxide subcaste (aluminum oxide, Al_2O_3) provides some position of protection against erosion and oxidation, which is salutary for the life of the device. These advantages make aluminum a favored choice for metallization in MOSFETs [17].

Chapter 6

DEVICE STRUCTURE AND FABRICATION

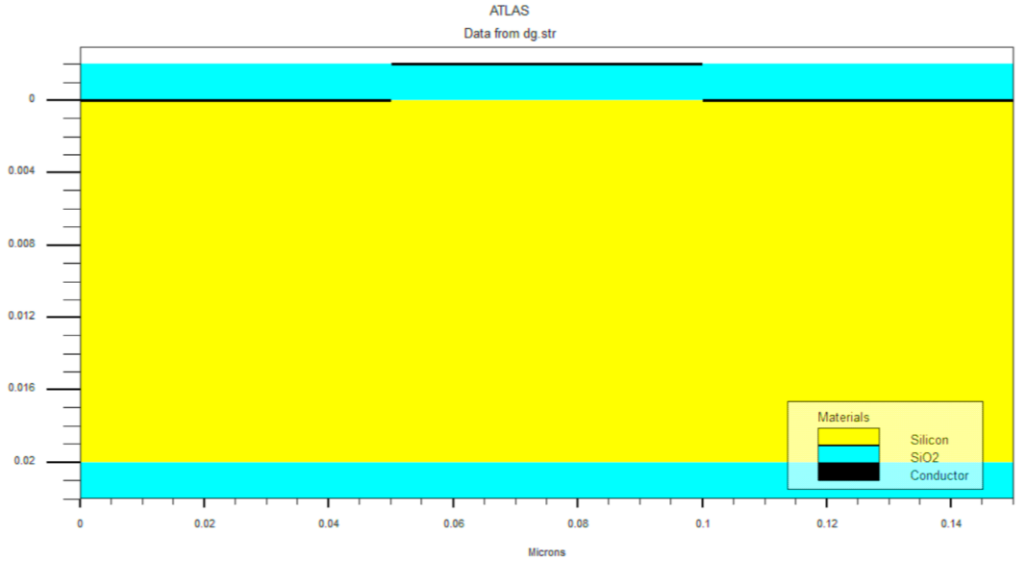
6.1 Present Trends in DG MOSFET Structure

The current advancements in Double Gate Metal Oxide Semiconductor Field Effect Transistor (DGMOSFET) structures are focused on improving device performance, scalability, and power efficiency in the context of ongoing miniaturization. Notably, there is a prominent shift towards FinFET and nanowire architectures. FinFETs, a type of DG MOSFET with the gate wrapped around a thin silicon fin, have become the industry standard for technology nodes below 22nm due to their superior electrostatic control, which effectively mitigates short-channel effects and reduces leakage currents. As device dimensions continue to shrink, nanowire FETs are gaining attention due to their gate-all-around (GAA) structure, providing even better electrostatic control by completely surrounding the channel. These architectural developments are crucial for preserving performance and reliability as transistors approach atomic scales. In addition to architectural innovations, material advancements are playing a pivotal role in the evolution of DG MOSFETs. The widespread adoption of high-k dielectrics such as hafnium oxide (HfO2) has been instrumental in addressing gate leakage issues, enabling the utilization of thicker dielectric layers without compromising capacitance. Furthermore, alternative channel materials such as germanium (Ge) and III-V compounds (e.g., InGaAs) are being explored to enhance carrier mobility and drive current, which are essential for high-speed and high-performance applications. Strain engineering, achieved through methods like epitaxial growth of SiGe or Ge, is also being utilized to enhance carrier mobility by introducing tensile or compressive strain in the channel. Coupled with sophisticated fabrication techniques such as atomic layer deposition (ALD) and advanced lithography, these trends are pushing the boundaries of DG MOSFET technology, positioning it as a cornerstone for next-generation electronic devices, ranging from ultra-fast processors to energy-efficient mobile devices.

6.2 Device Architecture

The equivalent capacitance model and the proposed device architecture (2D & 3D) are displayed in Fig. 6.1. This diagram displays the complete DG MOSFET construction. The lengths of the gate (L_G), drain (L_D), and source (L_S) are 150 nm, 50 nm, and 50 nm, respectively. Table: 1 lists the additional structural variables that were utilized in this architecture. They are quite logical and exact.

(a)



(b)

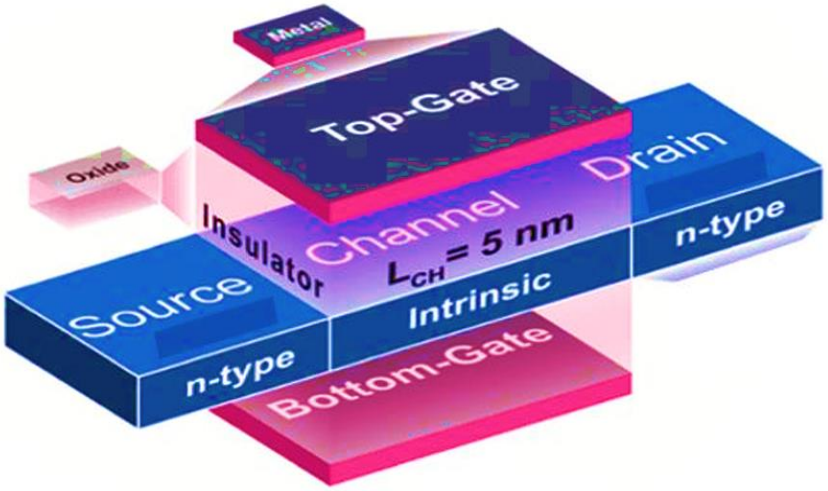


Fig 6.2.1: (a) Silvaco 2D outlook of silicon MOSFET with double gate (b) 3D view of the double gate MOSFET

Table 6.2.1: Parameters of the proposed DGMOSFET

Parameter Name	Value
Length of Gate	50 nm
Length of Drain	50 nm
Length of Source	50 nm
Dielectric constant of SiO2	25
Source Doping Concentration	1x1020/cm3(n-type)
Drain Doping Concentration	1x1020/cm3(n-type)
Channel Doping Concentration	1x1015/cm3(p-type)
Gate work Function	4.74 eV

(a)

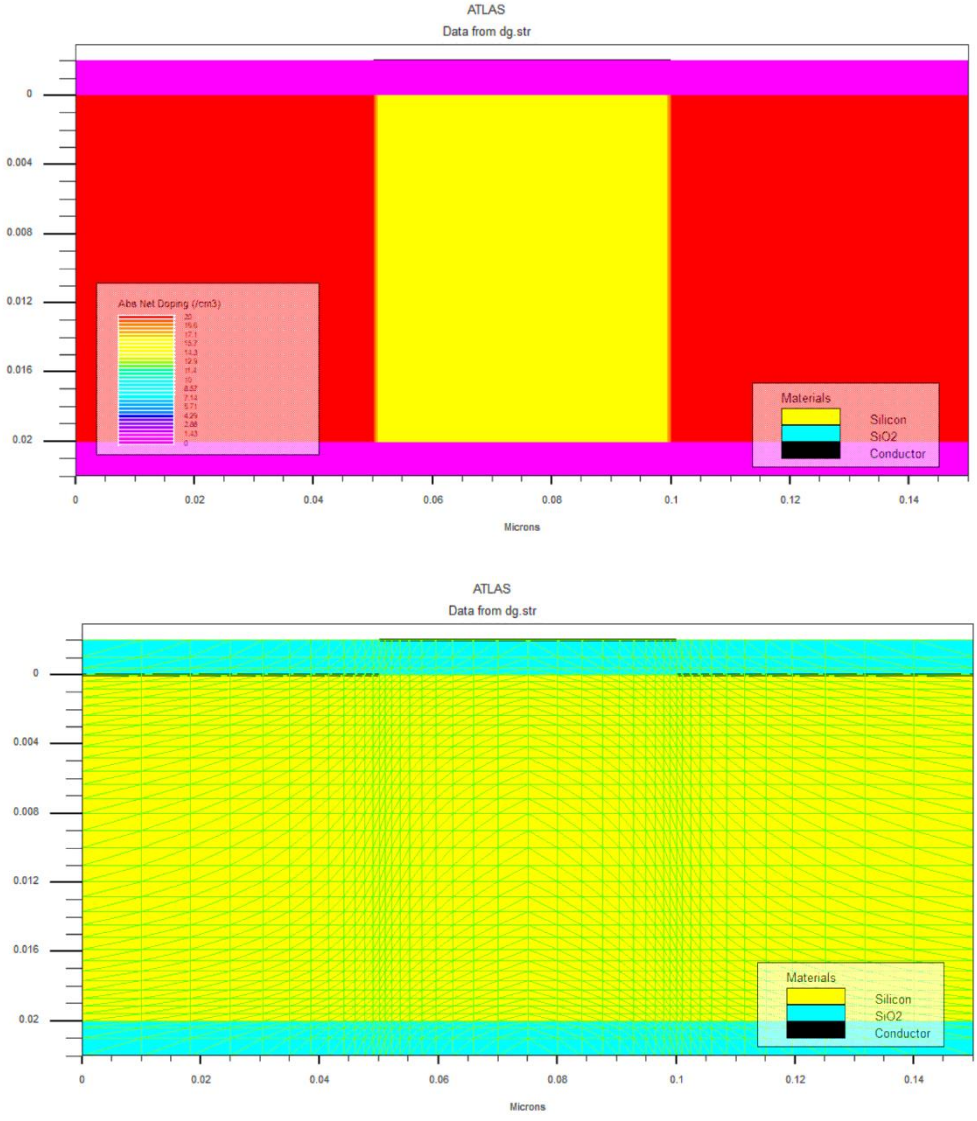


Fig6.2.2: (a) Doping profile & (b) Mesh Structure of the proposed DGMOSFET

Chapter 7

SIMULATION RESULT ANALYSIS AND DISCUSSION

7.1 Result Extraction

We've familiarized ourselves with the proposed structure of the Double Gate MOSFET design, armature, and simulation fashion in the former chapters. Now, after running the simulation a number of times in Silvaco Atlas with differing values, we will get affair angles and bias word in TonyPlot. From TonyPlot we can save the results as a CSV (comma- separated value) file, which we can compass using conniving software. We used OriginLab (Origin Pro) to plot out the affair lines and get the angles we bear for the evaluation of our DGMOSFET device.

7.2 Energy Band

The comprehension of the energy band diagram is imperative for the comprehensive understanding of the operational characteristics and efficiency of Double-Gate MOSFETs (DG MOSFETs) with SiO2 gate structures. In the context of DG MOSFETs, the energy bands are subject to the influence of the voltages applied to both gates, thereby establishing a notably enhanced level of electrostatic control over the channel as compared to single-gate MOSFETs. This advanced control mechanism serves to mitigate short-channel effects and facilitates superior scalability. The energy bands, under diverse gate biases, delineate pivotal operational modes—accumulation, depletion, and inversion—each characterized by discernible band bending and carrier distributions. Notably, during the inversion mode, substantial downward bending of the conduction band near the semiconductor-oxide interface culminates in the formation of a conductive channel. The SiO2 gate dielectric assumes a pivotal role in ensuring the establishment of a high-quality interface and robust gate control, which are consequential in determining the device's threshold voltage and overall efficiency. The utilization of numerical simulations to analyze these energy bands yields profound insights into the electrostatic potential and carrier dynamics, thereby offering invaluable guidance for the optimization of DG MOSFET design to achieve heightened performance levels.

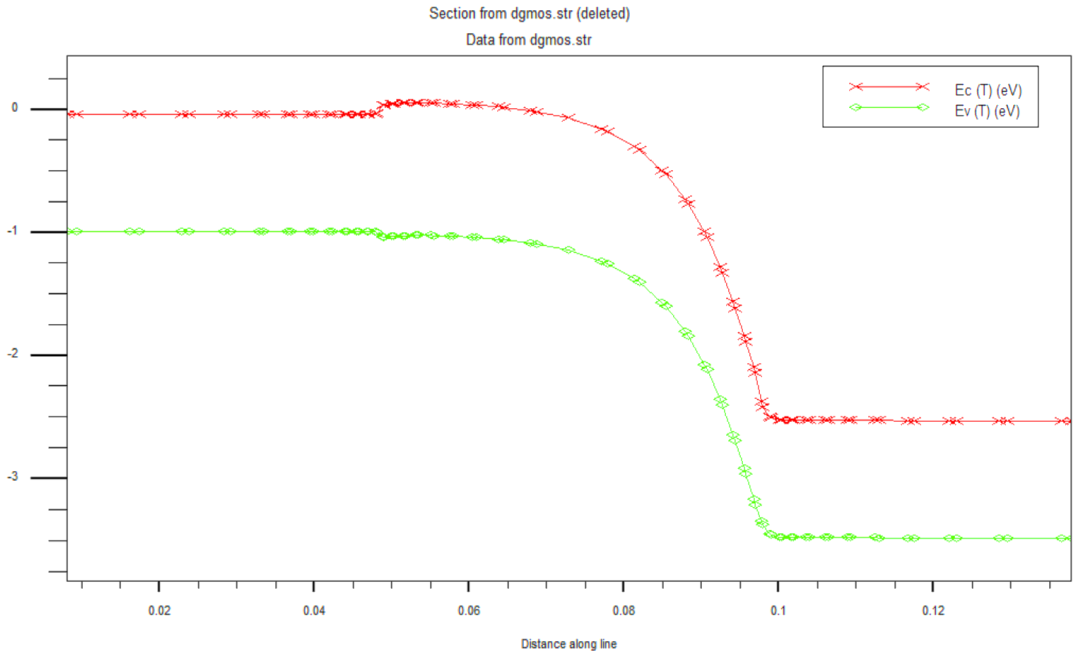


Fig7.2.1: Energy Band Diagram of DGMOSFET

7.3 Transfer Characteristics for DG MOSFET and I_{DS}-V_{DS} Characteristics Curve

In order to create an I_{DS} vs V_{GS} characteristics curve, one must first solve over the swept bias variable at each stepped point after collecting solutions at each step bias point. V_{GS} = 1.0 V is used to derive the V_{DS} values. These solutions' outputs are stored in.log files (solution files). The.log file is loaded, and ramping the gate voltage is done for each drain bias.

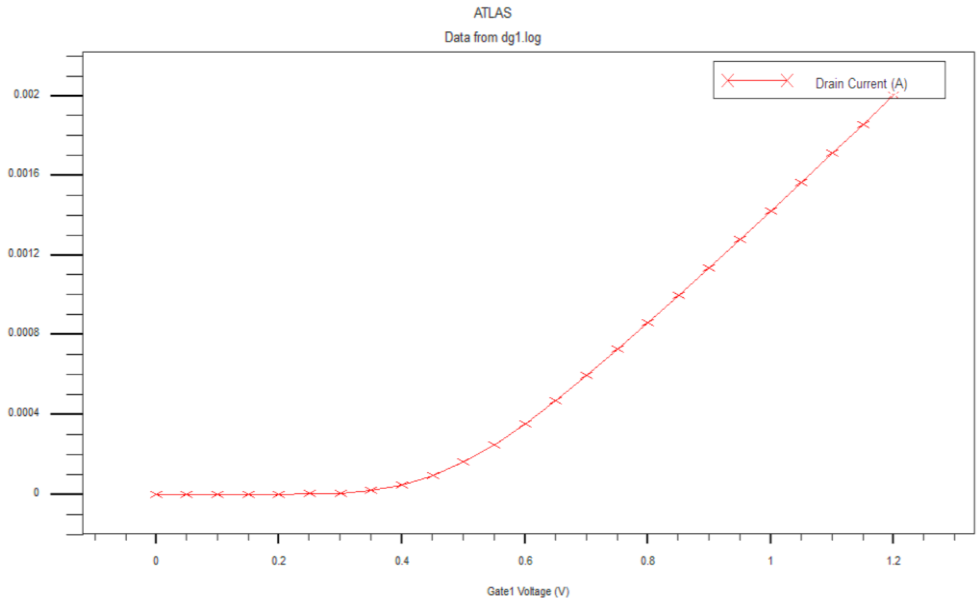


Fig 7.3.1. Transfer characteristics for DG MOSFET

While the gate voltage (V_{GS}) is scaled from 0 V to 1.0 V with a voltage step of 0.1 V, the drain voltage (V_{DD}) is fixed at 0.1 V. Finally, as illustrated in fig. 7.3. DG MOSFET, one I_{DS}-V_{GS} curve is superimposed using Tony Plot. In order to observe the current at conduction (inversion layer present) but at low electric field, V_{DD}= 0.1 V was selected.

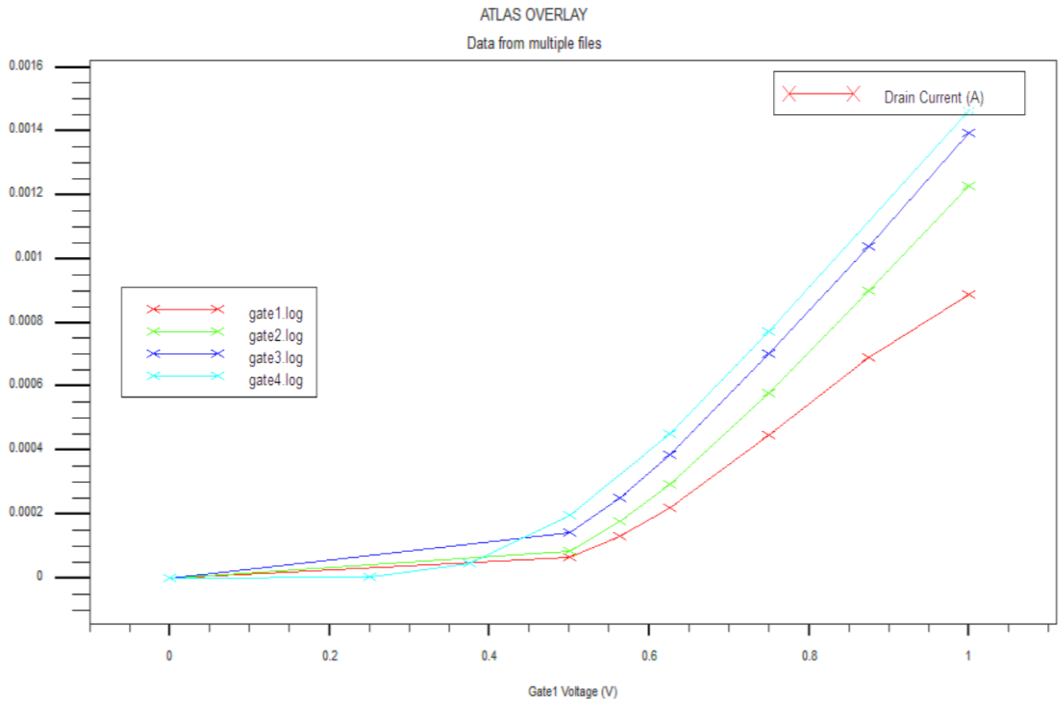


Fig7.3.3: I_{DS} vs V_{DS} of the DG MOSFET parameter for V_{GS}=0V, V_{GS}=0.5V, and V_{GS}=1.0V

Figure 7.3 displays the I_{DS} vs V_{DS} curves. In a DG MOSFET, the drain voltage (V_{DS}) is ramped from 0 V to 1.0 V by a voltage step of 0.1 V, while the gate voltage (V_{GS}) is set at 0 V, 0.5 V, and 1.0 V.

7.4 Sub threshold voltage, I_{OFF} & I_{ON} Current

Finding the threshold voltage, or VT—the gate voltage value at which a transistor becomes "ON"—and analyzing the I_{ON}/I_{OFF} ratio of on-off current are crucial. When I_{DS} is the lowest value and the Dirac point serves as the inversion point where hole conductance changes to electron conductance, VT is extracted. It can also detect the point at which gm (V_{GS}), or transconductance, equals zero. Consequently, when V_{DD} equals 0.1 V, VT is extracted, and a voltage step of 0.1 V is used to ramp the gate voltage from 0 V to 1.0 V. Drain current during transistor off-state, or I_{OFF}, occurs when the gate-to-source voltage (V_{GS}=0V) is zero. There are numerous factor can influent I_{OFF} such as VT, channel physical dimensions, channel / surface doping profiles, V_{DD}, gate oxide thickness, and the depth of the drain/source junction.

When a transistor is in the on state, an additional current known as I_{ON}—the maximum value of I_{DS}—flows between the source and drain. Given that VT and current are connected, this study also applies the formula V_{GS}-VT = 1V, which determines the precise value of I_{ON} in a typical MOSFET. Therefore, the value of the ION at bias V_{DD}=0.1 V and V_{GS}=1.0 V (maximum range) is taken here.

For V_{DD} = 0.1 V, VT is 0.107 V.

For DGMOSFET, I_{OFF} is 0.198 nA and

I_{ON} is 602 µA when V_{DD} is equal to 0.1 V.

The drain current varies with the gate-to-source voltage for two distinct Vds values. The subthreshold slope and the DIBL calculation are also displayed.

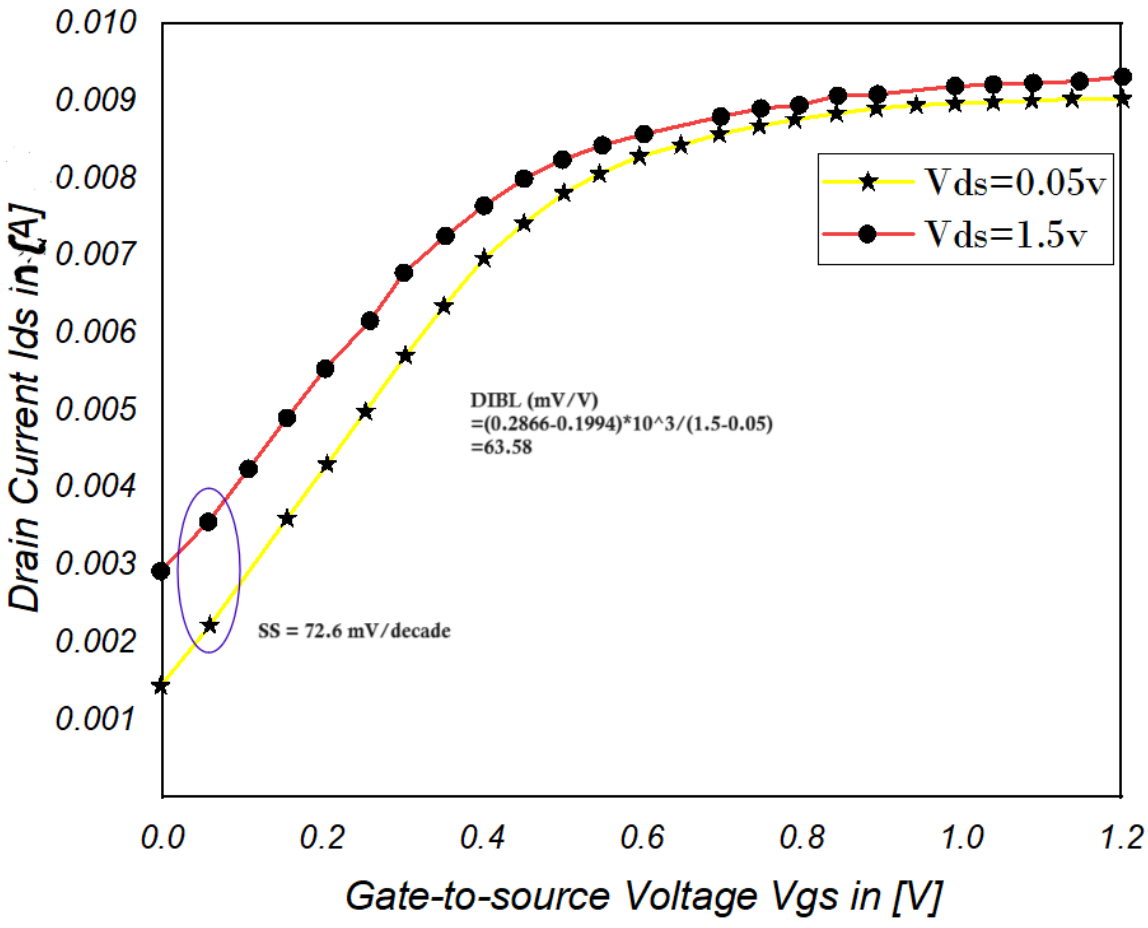


Fig 7.4.1: Schematic of DIBL calculation and Subthreshold slope

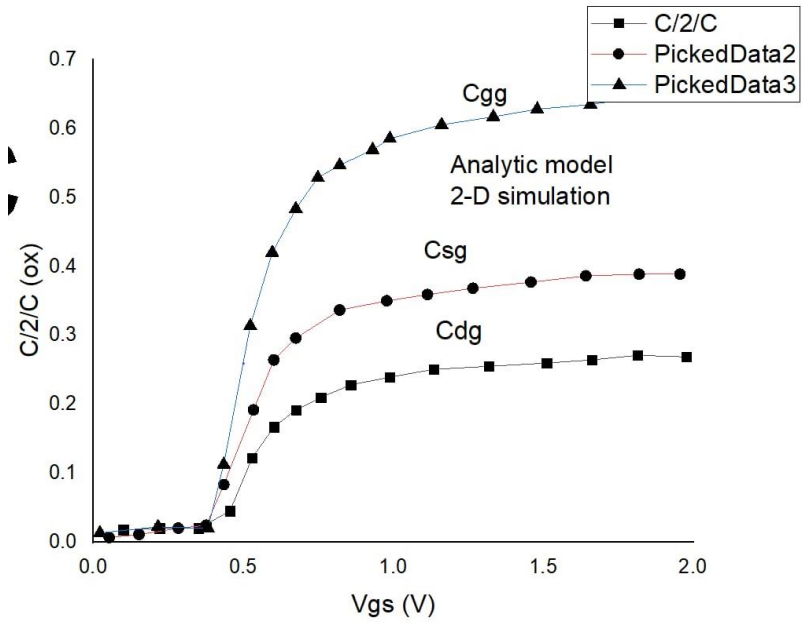


Fig 7.4.2: Shows the capacitances of a DG MOSFET (normalized to the oxide capacitance) as a function of gate voltage, comparing the findings of the 2-D numerical simulation with the analytical model.

The capacitances estimated by the analytical model correspond quite well with the numerical integration and simulation findings, as shown in Fig. 7.5. Because there are no additional approximations involved in the preceding derivation of the trans-conductance gm, gds, and current Ids necessary in, the capacitance model achieves similar precision as the charge model.

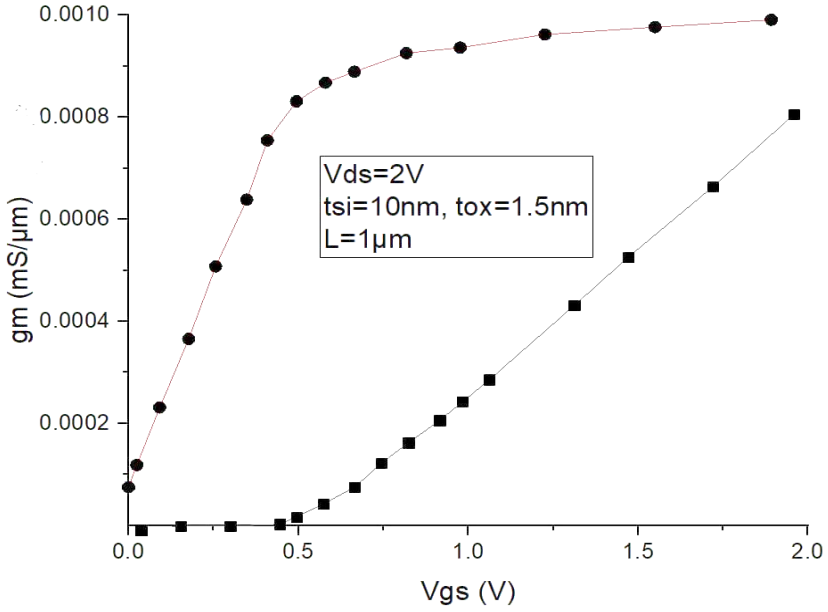


Fig7.4.3: Shows the transconductance gm on both the left and right logarithmic and linear scales, derived from the analytical model.

7.5 Simulation Results

The horizontally translated Ids-Vgs characteristics for low (Vds = 0.05 V) and high (Vds = 1.5V) are displayed in Figure 7.4. The number of millivolts of translation per volt change in drain voltage is what defines the translation, which is called DIBL. The DIBL in this instance is 63.58 mV/V, which is acceptable because well-designed MOSFETs usually have a DIBL of less than 100 mV/V. additionally, subthreshold swing (SS) is depicted in Figure 6.4. SS is defined as the number of millivolts of gate voltage rise required to raise the drain current by a factor of ten. It is represented by the slope of the Ids Vgs curve in the subthreshold region. The acceptable value of SS for well-designed MOSFETs is less than 80 mV/decade in order to enable a quick transition between the off and on states (i.e., a small SS). The theoretical lower limit of SS is 60 mV/decade at ambient temperature.

7.6 Summary

A thorough introduction to MOSFET simulation using Silvaco TCAD tools is provided in this chapter. The focus is on the approach and process used to simulate MOSFET devices with Silvaco. Additionally given is a summary of the software Silvaco created to satisfy the simulation requirements for studying both traditional and cutting-edge MOSFET architectures. Furthermore, a number of source code samples are included for the task of emulating various MOSFET varieties that are in use today. It was demonstrated how utilizing Silvaco TCAD to simulate devices can provide a unique perspective on MOSFET behavior.

Chapter 8

CONCLUSION AND RECOMMENDATIONS

8.1 Conclusion

In summary, a double gate MOSFET structure is demonstrated by combining a Silicon dioxide (SiO2) in the gate stack with a Si baseline FET. When it comes to fabricating high-performance bias for low-power operations, DGMOSFET is showing incredibly promising results, just when CMOS scaling is reaching its limits. Its contributions have yielded significant insights on the capabilities and implicit improvements related to semiconductor bias.

Electrostatic control over the channel was much improved by the two gate armature, which decreased short-channel problems and improved device performance. Advanced driving currents (I_{ON}) and a lower off-state current (I_{OFF}), which are essential for low-power operations, were obtained with this arrangement. Through implicit alteration within the DGMOSFET channel armature and band-to-band tunneling optimization, ferroelectric gate insulator adjustment can improve the I_{ON}/I_{OFF} rate. Optimizing the gate dielectric by colored ferroelectric accessories can greatly increase the I_{ON}/I_{OFF} rate by improving band-to-band tunneling control and implicit modification. With a 2 nm silicon dioxide in the gate stack, the lowest SS of 60 mV/dec is reached, indicating the potential for this MOSFET structure as energy-efficient switches. By entirely encircling the MOSFET, the suggested SiO2 nanowire gate reduces power consumption and eases scale down constraints.

As a result, Si/SiO2 Double Gate MOSFET seems like a promising technology for an Internet of Things (IoT) platform, offering a unique route for the ongoing growth of the use of electronic devices.

8.2 Future Recommendations

To find out more about the actual performance of this Numerical Investigation of Double Gate Metal Oxide Semiconductor Field Effect Transistor with SiO2 Gate Structure, the following features can be examined:

- Investigation of different electrostatic integrity, current drive efficiency, and thermal management.
- Automotive, industrial and communications systems.
- Integration with existing technologies.

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APPENDIX A

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