Design of N^{th} Level Inverter using Asymmetric H-Bridge MLI Topology:
With Techniques to Minimize THD

A Project report is submitted in partial fulfillment of the requirements for the award of Degree of Bachelor of Science in Electrical and Electronic Engineering.

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DECLARATION

I hereby declare that this project "**Design of N-th Level Inverter using Asymmetric H-Bridge MLI Topology: with Techniques to Minimize THD**" represents my own work which has been done in the laboratories of the Department of Electrical and Electronic Engineering under the Faculty of Engineering of Daffodil International University in partial fulfillment of the requirements for the degree of Bachelor of Science in Electrical and Electronic Engineering, and has not been previously included in a thesis or dissertation submitted to this or any other institution for a degree, diploma or other qualifications. I have attempted to identify all the risks related to this research that may arise in conducting this research, obtained the relevant ethical and/or safety approval (where applicable), and acknowledged my obligations and the rights of the participants.

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APPROVAL

The project entitled **"Design of Nth Level Inverter using Asymmetric H-Bridge MLI Topology: with Techniques to Minimize THD"** submitted by **Ubaidur Rahman (I201-33-1132), Md Iftekhar Haque (201-33-1231), Md Sazzadul Alam (201-33-1292) & Md Sabbir Ahmed (201-33-1267)** has been done under my supervision and accepted as satisfactory in partial fulfillment of the requirements for the degree of **Bachelor of Science in Electrical and Electronic Engineering** in **February, 2024.**

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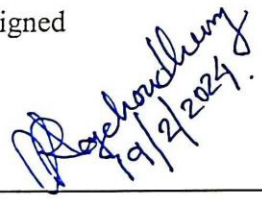

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Dedicated

To

Our Beloved Parents

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LIST OF ABBREVIATIONS

AC	Alternating Current
APODPWM	Alternative Phase Opposition Disposition Pulse Width Modulation
ASHB	Asymmetrical H-Bridge
BPDB	Bangladesh Power Development Board
BERC	Bangladesh Energy Regulatory Commission
CHB	Cascaded H-Bridge
CHBMLI	Cascaded H-Bridge Multilevel Inverter
DC	Direct Current
DCLR	DC Link Ratio
DE	Differential Evolution
EMC	Electromagnetic Compatibility
FACTS	Flexible Alternating Current Transmission Systems
FC	Flaying Capacitor
GA	Genetic Algorithm
HVDC	High Voltage Direct Current
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IPP	Independent power producer
MLC	Multilevel Converter
MLI	Multilevel Inverter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NPC	Neutral Point Clamped
OVL	Output Voltage Level
PSO	Particle Swarm Optimization
PWM	Pulse Width Modulation
SHE	Selective Harmonic Distortion
SREDA	Sustainable and Renewable Energy Development Authority
THD	Total Harmonic Distortion

LIST OF SYMBOLS

Symbol	*Name of the symbol*
C	Collector
$\frac{dv}{dt}$	Rate of Change of Voltage
E	Emitter
G	Gate
H_z	Frequency in Hertz
L	Inductive Load
L_{max}	Maximum Number of Output Voltage Levels
N	Number of H-bridges
N_L	Number of Output Voltage Level
R	Resistive Load
S_n	*n*-th Switch
S_r	Sum of Voltage Source Ratios
V	Voltage
V_{DC}	DC Voltage
V_{Hn}	n-th H-bridge Voltage
V_{out}	Output Voltage

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ABSTRACT

The Asymmetrical H-Bridge (ASHB) Multilevel Inverter (MLI) is an advanced power electronics device, gaining notable interest for its capacity to efficiently convert high power while minimizing harmonic distortion. This research paper extensively explores the Asymmetrical H-Bridge Multilevel Inverter, delving into its operational principles, distinctive structure, and inherent advantages compared to standard two-level inverters, providing valuable insights into its potential applications in power conversion systems. We begin by describing the Asymmetrical H-Bridge Multilevel Inverter's architecture, which consists of cascaded H-bridge modules capable of generating multiple voltage levels, leading to improved voltage output resolution. We propose an equation to construct the N-th level of the Asymmetrical H-Bridge Multilevel Inverter, enabling engineers to synthesize higher-level inverters tailored to specific application requirements. The equation takes into account the number of H-bridge modules necessary for the desired level and ensures precise voltage level generation. Additionally, we present a novel approach targeted at mitigating Total Harmonic Distortion (THD). Our method incorporates two distinct techniques, and one of the pivotal components is the introduction of a proposed voltage ratio. As a consequence of this innovation, we have achieved a significant reduction in THD, obtaining a remarkable value of 2.89% over a spectrum of 39 levels. A comprehensive investigation of the Total Harmonic Distortion (THD) is undertaken, emphasizing the Asymmetrical H-Bridge Multilevel Inverter's capacity to attain low THD values, which considerably increases the quality of the output voltage waveform.

Keywords: Asymmetrical H-Bridge (ASHB), Multilevel Inverter (MLI), Total Harmonic Distortion (THD), Nth Level Construction, Power Electronics, Output Voltage levels.

CHAPTER 1
INTRODUCTION

1.1 Background

In contrast to traditional machine drives that utilize two- or three-level inverters, cascaded H-bridge (CHB) multilevel drives now exhibit significantly reduced distortion. The primary objective is to use low- or medium-voltage devices to create converters that efficiently handle higher power levels at elevated voltages. Multi-level converters (MLCs) are currently being adopted in various industries, such as motor drives, HVDC, and FACTS (Flexible AC Transmission Systems), as well as in the integration of renewable energy sources. This innovative approach has the potential to revolutionize electricity infrastructure and accelerate the utilization of renewable energy. Extensive research has led to the discovery of several topological modifications, such as diode clamping, flying capacitors, cascaded H-bridges, and other hybrid versions. These diverse topologies offer a wide range of design and implementation options for multi-level converters, catering to different application requirements and performance objectives. Among these options, the cascaded H-bridge Multi-level Converter (MLC) stands out for its simple design and minimal control requirements. Nonetheless, many other topologies face the significant challenge of maintaining capacitor balance. The introduction of a hybrid topological concept is notable as it addresses this crucial issue and offers a viable solution.

1.2 Problem Statement

Presently, a comprehensive equation does not exist for determining the maximum or minimum output levels achievable through Asymmetrical H-Bridge MLI inverters based on the DC link ratio. Additionally, there is a lack of elucidation regarding the Total Harmonic Distortion (THD) associated with these output levels when utilizing such an equation. The absence of a detailed description exacerbates the challenge of understanding the intricacies of these inverters and their performance characteristics in relation to DC link ratio and THD.

There is a noticeable absence of information pertaining to critical aspects such as the number of switches employed, the anticipated output magnitude, the specific configuration of the switching mechanism, the resultant output levels upon

implementation, and the consequent power quality in terms of Total Harmonic Distortion (THD). The lack of details in these crucial areas hinders a comprehensive understanding of the operational characteristics and performance attributes associated with the system in question.

The discussion surrounding the reduction of Total Harmonic Distortion (THD) below the IEEE standard encompasses a variety of techniques that have not been thoroughly explored. Specifically, the potential improvement in signal quality by lowering THD to 2.89% from its current state below the 5% threshold has not been adequately addressed. There exists the possibility of enhancing signal quality through such reduction methods, yet a comprehensive examination of this aspect has been notably absent from the discourse. Exploring and deliberating on these techniques could potentially offer valuable insights into optimizing signal quality beyond the established IEEE standard.

1.3 Objectives

Multilevel converters offer the advantage of producing output voltages characterized by minimal distortion while simultaneously mitigating the stresses associated with $\frac{dv}{dt}$ (rate of change of voltage). This dual capability holds significance in the realm of electromagnetic compatibility (EMC) as it contributes to the reduction of potential issues related to electromagnetic interference. In essence, the utilization of multilevel converters not only enhances the quality of output voltages by minimizing distortion but also contributes to an overall improvement in electromagnetic compatibility by curbing the undesirable effects of $\frac{dv}{dt}$ stresses.

Multilevel converters, a specialized type of power electronic converters, possess the ability to draw in the input current while ensuring a minimal level of distortion. This essentially means that these converters can manage the input current in a manner that the waveform remains largely undistorted, maintaining its original form. This is a significant advantage as it ensures the efficient operation of the system connected to these converters, reducing the risk of potential damage caused by distorted currents. Therefore, the use of multilevel converters contributes to the overall stability and reliability of the power system.

In terms of switching frequency, multilevel converters have the flexibility to operate at both fundamental switching frequency and high switching frequency Pulse Width

Modulation (PWM). It's important to note that a lower switching frequency typically results in lower switching loss and consequently, higher efficiency. This is a key factor in the performance of these converters and contributes to their widespread use in various applications.

Furthermore, the output waveforms of the voltage and load current produced by multilevel converters are also approximated sine waves. This means that the output closely resembles a smooth, continuous sine wave, which is ideal for many electrical systems. This feature of multilevel converters ensures better performance and reduces the risk of damage to connected devices due to irregular waveforms.

Lastly, one of the key advantages of multilevel converters is the ability to increase the number of voltage levels in the inverter without requiring a higher rating on individual devices. This can lead to an increase in power rating. This feature allows for greater flexibility in system design and can contribute to improved system performance and efficiency. In summary, multilevel converters offer several advantages in terms of input current management, switching frequency, output waveform quality, and power rating, making them a valuable component in many power systems.

1.4 Brief Methodology

At the very beginning of our research, we were curious about the power quality that we are receiving from BPDB and IPPs. Therefore, it deals with the reduction of total harmonic distortion after we go through the research findings and start our literature survey. From all kinds of research methodology, we have mostly used quantitative research. We tried our best and we found two techniques to reduce the total harmonic distortion of the Inverses. We have compared the results obtained in technique I & II and their combination.

Through them, we have given our conclusion about what best we can achieve through this technique. To accomplish this task we used three types of research methodology. Then we started our work on the technique on the methods that may research have already been implemented to improve the Quality of power and we found The Multilevel Inverter plays a big role and they have a Big Contribution to the Improvement of Power Quality. So we State our findings on the type of MLIs we find that there are two or three types of MLIs and we see Asymmetric H Bridge MLIs will help us at the goal and we use the fundamental research type of methodology.

After going through the method, we know how to analyze the voltage level gap, how the switches work, and how we can get to our goal. Once we reach our goal then we reach our goal then we have standardized that what are the outcomes of those techniques and what are the improvements that we may techniques I & II and also the combination of both techniques. We have standardized how minimum the THD we can achieve these three Methodology. We have used during our total research period.

1.5 Gantt Chart

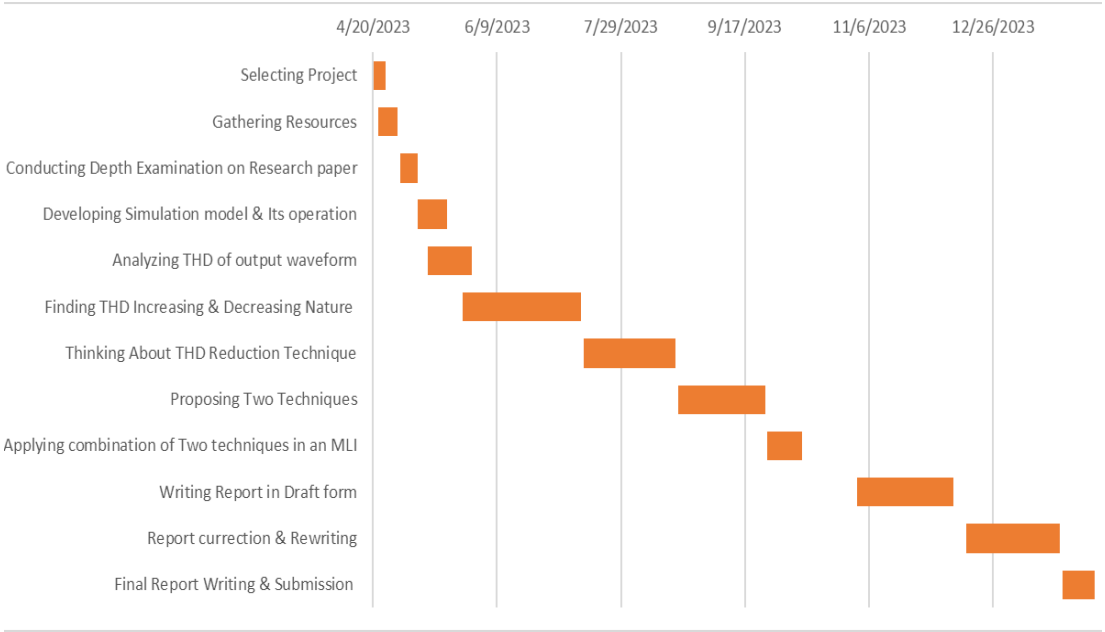


Figure 1.1: Gantt chart of Implementation Schedule

1.6 Structure of the Report

In Chapter 1, the background section of the study sets the stage by providing context, emphasizing significance, and identifying any research gaps. The problem statement pinpoints issues, while goals are outlined in the objectives, and the methodology explains the research approach. The implementation schedule ensures efficient project oversight. Moving to Chapter 2, the literature review plays a crucial role in any research, offering existing knowledge on the issue and paving the way for advancements. It helps identify errors, contradictions, and areas for further study. Chapter 3 delves into system design, involving the analysis and arrangement of software, file storage, and graphical interfaces to achieve desired outcomes. Design analysis evaluates the impact, identifies potential issues, and ensures the system meets requirements. Chapter 4 focuses on presenting the actual findings of the study,

encompassing data, simulations, and observations. It provides an objective perspective, including statistical analyses and qualitative findings. The aim of the thesis is to elucidate the significance, impacts, and potential limitations of the outcomes. Within Chapter 5, there is an extensive overview of the project, including its schedule, resource use, methodology, results, lessons learned, suggestions, and information on the project's progress, research techniques, outcomes, and initiatives for the future. Chapter 6 highlighted how the high efficiency of the inverter enhances user experience, minimizes consumption of energy, and addresses power quality issues. It offers a sustainable solution and minimizes the need for filter circuits by reaching IEEE standards. In Chapter 7 examines the Asymmetrical H-Bridge Multilevel Inverter (ASHB MLI) as a sustainable and economically feasible high-power approach. It aims to minimize Total Harmonic Distortion and provides recommendations for future applications and the advancement of technology in this area of study.

CHAPTER 2
LITERATURE REVIEW

2.1 Introduction

This thesis paper aims to design an Nth-level Inverter using an Asymmetric H-bridge MLI topology with the techniques to minimize total harmonic distortions. Inverter is mostly used in contemporary technology for various works. Multilevel inverter focused on minimizing the count of switches and sources while maintaining the output waveform in the acceptable range of total harmonic distortions. This helps mitigate the overall costs and other losses. The cascade H-bridge stands out as a compelling choice for a renewable system. If we look for renewable energy sources, the output power of this system contains harmonics which decrease the output quality. H-bridge Inverter can mitigate this problem and increase the output quality by reducing the harmonic distortion. This work is mainly work on how to solve this issue of harmonics and can invert multilevel. While attempting to complete this work, a literature review was conducted. Because trying to figure out the related topics and related works where the design can be implemented for the multilevel inverter, then compare this work with other literature and find the limitations of present works that were published on different platforms.

2.2 Related Research

Electronic devices recognized as inverters play a role in transforming electrical energy that is direct current (DC) into alternating Current (AC). This is done by the use of semiconductor switches such as MOSFET, IGBT.

According to a study on inverters have emerged throughout time to meet increasing requirements for power conversion for modern applications. The first invented inverter is known as a conventional inverter. This inverter, which has voltage levels of +V and -V, generates an output voltage or current in just two levels; it can be referred to as a two-level inverter. High power and high voltage applications are rated for this inverter, which runs at a high switching frequency and with substantial power loss [1]. One of the main causes of the inadequate output quality of this conventional inverter is harmonic distortion. This makes it challenging to directly integrate power electronics

switches with medium- and high-voltage grids. A multilevel inverter was developed as a solution to these shortcomings of conventional inverters.

Another study was done on the output of the multilevel-inverter (MLI) over the conventional inverter [2]. To meet the substantial demand for low and medium-power applications, multilevel inverters (MLIs) are preferred as they can boost output voltage without employing transformers [3, 4]. Primarily, these inverters were employed for low-volume uses, like supplying relatively small electrical devices or electronic devices. Due to increasing power needs and renewable energy popularity, multilevel-inverters (MLI) were developed to enhance the high quality of power output and system flexibility [5]. Additionally, it has excellent quality of power waveforms with minimum distortion, higher voltage and power quality and lower switching losses. Multilevel inverters develop output voltage in small levels, which evaluate the inverter level [6]. While conventional inverters produce binary waveforms, multilevel-inverters (MLI) can generate voltage waves consisting of multiple discrete voltage levels. To create a sinusoidal AC voltage, a multilevel inverter requires numerous DC voltage sources and transforms them into one level of AC voltage. However, it can become in proximity to sinusoidal waves with harmonics, which makes the staircase form change abruptly. Therefore, the inverter to enhance the efficiency of AC power, which leads to reduced harmonics, utilizes small conversion of power steps.

As per the further study, cascaded H-bridge (CHB) technology is significantly more prevalent than floating capacitor (FC) and neutral point clamped (NPC) in various topologies of multilevel inverters (MLIs). This is mainly due to its balanced DC voltage source and its significance it requires the fewest components to design a modularized circuit. But, electrical devices need a uniform sinusoidal waveform, such topologies build distorted output waveforms. According to IEEE-519 (2014), a smooth sinusoidal waveform requires a total harmonic distortion (THD) value < 8% [7]. In cascaded H-bridge multilevel inverters, distinct DC source is contained across each H-bridge and using controlling the switching angles of switch may enhance power quality and reduce THD. Based on n input of the number of independent DC sources, cascade multi-level inverters provide output phase voltage is $2n+1$ [8]. However, this presents a constraint that can be resolved by adding a flying capacitor into the CHB and utilizing asymmetrical DC power supplies [7]. There are numerous DC sources and an unbalanced voltage source, the asymmetric H-bridge is more often used over the

symmetric H-bridge is discussed [9]. Moreover, the harmonics were decreased [10]. In asymmetric systems when binary and trinary systems are utilized to provide more levels in the output with minimal switches, symmetrical systems are employed to create tolerant systems [11, 12]. APODPWM (alternate phase opposition disposition pulse width modulation) has 1.79% more harmonics than the asymmetric three-phase cascade PDPWM (phase disposition pulse width modulation) approach, which has 1.75% less harmonics [10].

According to another study on the concerning power quality, one of the most significant issues is- cascading inverters aim to reduce the number of power switches to minimize the total harmonic distortion (THD) of the waveform of the output voltage. Numerous methods exist to reduce harmonic distortion such as numerical series technique, selective harmonic elimination (SHE). In numerical series technique, a substantial decrease in total harmonic distortions (THDs) was observed in the study, which measured a range of multilevel waveforms, including 9-level, 11-level, and 13-level [13]. But, in high-power applications with lower switching frequency needs, SHE prevails. In this case, a seven-level cascade inverter's approach of finding three switching angles that cancel out two harmonics is explained along with a newly devised SHE for graphical analysis. 5th and 7th harmonics may be eliminated using three switching angles [14, 15].

In access to reducing the power switch in a multilevel inverter, different technological approaches have been utilized these approaches enhanced the inverter's efficiency, reliability, and cost-effectiveness while simultaneously keeping the intended output waveform. To enhance the functionality of a single-phase cascaded multilevel inverter beyond its previous limitation of generating purely positive levels, an additional DC voltage source is integrated with four H-bridge switches and two unidirectional switches. [16]. Further, an alternate MLI structure generates 17th levels with a total harmonic distortion of 5.79 % using a combination of four asymmetric sources and six switches [17]. Adding a high pass filter allows for a reduction of 2.02%, which meets the IEEE-519 standard. Furthermore, the THD was found to be 80.23% and 29.01%, respectively, for the two-level inverter with and without PWM method in [18]. In the instance of a multi-level inverter, the total harmonic distortion (THD) reached 26.60% when using the PWM approach and 28.95% when not applying it.

The issue emerges in the direct connection of a single semiconductor switch in a medium voltage range grid (KV range) while addressing the H bridge cascade MLI design. We focus on high voltage and high switching frequency on the grid in the megavolt range [19]. Low voltage and low switching frequency level harmonics are the cause of the complexity. After solving non-linear transcendental equations, selective harmonics reduction pulse width modulation (SHEPWM) is the most practical modulation approach to reduce the designed low level of harmonics among all the other pulse width modulation (PWM) techniques [20-22]. Low-frequency harmonic distortion can be effectively treated with the selective harmonic elimination (SHE) approach. However, there are still certain obstacles to overcome, such as choosing suitable initial gausses and computing derivatives for each iteration that caused divergence in the solution and singularity difficulties [23, 24]. Certain swarm optimization (PSO), modified PSO, genetic algorithm (GA), differential evolution (DE), grey wolf optimization, and other contemporary techniques are applied in response to these issues. All the solutions to the SHE equations may be found using algebraic equations; nevertheless, this method is only applicable for a limited number of switching angles because the switching angle grows with a polynomial degree [25]. Hence the authors from [26] proposed a novel method termed the homotopic perturbation method (HPM) to compute the SHE-PWM switching angles.

The application-based research in a nine-level inverter-based open-end induction motor drive that utilizes two asymmetric DC supplies is addressed [27]. It eliminates the possibility of overcharging the smaller DC bus, keeps the floating capacitors well-balanced irrespective of the switching frequency, modulation index, or load current, and focuses on the selection of space vectors which ensure that both DC sources continuously supply actual power to the load. This structure that has been developed is appropriate for use in applications such as electric vehicle traction and industrial drives. Additionally, a system is put in place that is suitable for electric vehicle applications and FACTs [28]. This approach relies on a CHBMLI with three voltage sources, 12 switches, and a THD of 3.77% for the 27 levels, which leads to reduced power losses and an efficiency of 92.38% [29].

2.3 Compare and Contrast

The author [4] provided a suggested transformer-based MLI topology (TBMLI) with reduced components. Using a 9L basic construction, experimental aspects were experimented. THD is now the primary issue with H-bridge MLI, and many researchers are working to lower THD. In this study [6], the author decreased the overall harmonic distortion in the cascaded H-bridge MLI from 23.41%, 21.85%, 20.57%, and 17.06% at the 7-level, 9-level, 11-level, and 13-level, respectively. They employed a total of twelve switches in this study instance. The author [7] conducted additional research and came to different conclusions for CHB, NPC, and FC topologies. The THD was 26.97% utilizing a hybrid modulation approach with a 5-level asymmetric MLI, according to results based on the CHB topology. The percentage of THD was 8.95% when there were nine levels. By using 8 power electronics switches rather than 28 switches, the author experimented with the 5-level MLI and found that the THD was the same. In order to increase power quality, the author [8] is very focused on minimizing THD to the lowest possible level. The outcome was a modulation index of 0.80 and V_DC=100V. The THD for 9-levels was 25.37% and for 11-levels was 7.05% by changing the switching angles. Additionally, they tried to lower SHE by changing the firing angles. Another study using a novel hybrid modulation method was conducted [10]. The inverter performance is calculated using PDPWM and APODPWM methods based on the experiment findings. The PD approach is less harmonic than the APOD method when the modulation index is changed from 0.7 to 1.0. THD from PD was 4.3%, 3.59%, 2.62%, and 1.75% when the modulation index was 0.7, 0.8, 0.9, and 1.0. APD was 4.28%, 3.57%, 2.70%, and 1.79%. The work was done using two H-bridge cells fed by two transformers with different turn ratios using the numerical series technique [13]. The mismatch in the turn ratios of the two transformers resulted in a research gap, which is why it was challenging to determine the number of levels. The output was then acquired using the Fast Fourier Transform (FFT) and the THD results without filter, which came out to 4.79% as opposed to the 8.99% that was predicted. The SHEPWM approach was used to minimize the lower-order harmonics [19]. They suggested that their SHE topology was viable for all modulation index values and that the fifth harmonics should become zero, but that SHEPWM should not be feasible for all values of the modulation index and that the fifth harmonics should be dominated.

However, this paper's limitations stemmed from the fact that the switch count was not reduced.

Above all, the current technology is examined and shown to have several shortcomings; for this reason, the suggested topology is unreliable. In order to lessen these current technology constraints, these specific topics are our primary focus. Our primary concerns are that the power quality should be high, with little THD and fewer switches. While the current technologies are limited to certain levels, we offered our approaches for Nth-level asymmetric MLI, allowing engineers to synthesize higher-level inverters adapted to specific application requirements. While the current working technology does not specify the precise voltage level generation, our proposed technique takes this into account and ensures precise voltage level creation by counting the number of H-bridge modules required for the desired level.

We also concentrated on THD mitigation. Level jump and level repetition are two separate approaches that we use in our approach. With the help of this method, we were able to significantly lower THD and acquire an impressive figure of 2.89% throughout a range of 39 levels. The majority of researchers find it difficult to operate with 39 levels and reduce THD in this proportion. We worked on the Nth level, and by increasing the number of levels, users can improve their voltage quality and THD. The current technologies only function at a limited number of levels, and the THD percentage is only valid for this specific level. So, the two main problems in asymmetric H-bridge MLI are the low output power quality and THD is reduced on our new technology and dominates the current MLI technology.

In this research work, we were trying to reduce the harmonics below 1%, but we could not achieve it. This situation is highlighted as a research gap, and we recommend the appropriate application of these two techniques to achieve harmonics below 1%.

2.4 Summary

A study of the literature on various types of multilevel inverter topology, which leads to several topologies and approaches, is included in this chapter. Reduced harmonic distortion, reduced voltage stress, higher power applications, improved efficiency, flexibility and scalability, grid integration, voltage support and management, and other factors led to the proposal of multilevel inverter topology above two-level inverter topology. This chapter covered the many harmonic reduction techniques that have been developed. The primary goal is to minimize THD and switch usage. Different methods, like SHE-PWM, GA, and PSO, are used to reduce THD and switching count, depending on the frequency of switching. All of this was covered in this chapter of the references article.

CHAPTER 3
MATERIALS AND METHODS

3.1 Introduction

As highlighted in the preceding portion, the imbalance in the DC link has a notable impact on the quantity of output voltage levels (OVLs) within the multilevel inverter (MLI) configuration of Asymmetrical H-bridges (ASHB). The manipulation of the DC link ratio (DCLR) emerges as a pivotal factor, enabling the augmentation or reduction of the OVL count.

In the subsequent discussion, we will delve into the intricate dynamics that transpire when two, three, and four asymmetric H-bridges (HBs) are consecutively linked. Concurrently, our endeavor is to elucidate the pivotal aspects governing the attainment of the maximum OVLs achievable in this cascaded setup and to discern the requisite DC link ratio (DCLR) for optimal functionality.

3.2 System Design for Various Case Study

Case 01: Maximum OVLs with Cascading Two ASHB

In the subsequent Cascading two HB where two voltage sources or two DCLR differ by a factor of 1:2. Two HB are linked together in series in **Figure 3.1**, and each HB has four switches. Switches $\mathbf{S_1}$, $\mathbf{S_2}$, $\mathbf{S_3}$ and $\mathbf{S_4}$ make up the first HB, and their output voltage is $\mathbf{V_{H1}}$. The second HB has switches $\mathbf{S_5}$, $\mathbf{S_6}$, $\mathbf{S_7}$ and $\mathbf{S_8}$, and its output voltage is $\mathbf{V_{H2}}$. Due to the series connection of two HBs, the overall output voltage is

$$V_{out} = V_{H1} + V_{H2} \quad (1)$$

Different on-off configurations of switches$\mathbf{S_1, S_2, S_3, S_4, S_5, S_6, S_7}$ and $\mathbf{S_4}$ are used in various combinations to produce different OVLs.

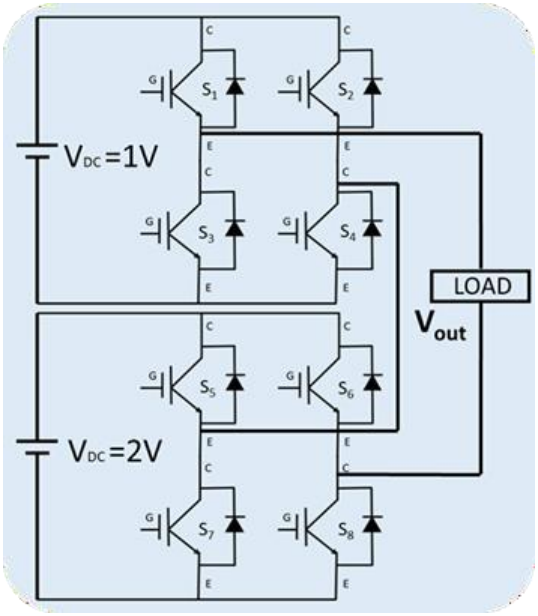


Figure 3.1: Cascading two HB with 1:2 DCLR

Level of voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
0V	1	1	0	0	1	1	0	0
	1	1	0	0	0	0	1	1
	0	0	1	1	1	1	0	0
	0	0	1	1	0	0	1	1

(a)

Level of voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1V	1	0	0	1	1	1	0	0
	1	0	0	1	0	0	1	1
	0	1	0	1	1	1	0	0
–1V	0	1	1	0	1	1	0	0
	0	1	1	0	0	0	1	1
	1	0	0	1	0	1	1	0

(b)

Level of voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
2V	1	1	0	0	1	0	0	1
	0	0	1	1	1	0	0	1
–2V	0	0	1	1	0	1	1	0
	1	1	0	0	0	1	1	0

(c)

Level of voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
3V	1	0	0	1	1	0	0	1
-3V	0	1	1	0	0	1	1	0

(d)

Table 3.1: Switching combinations for: (a) voltage level "0"; (b) voltage levels "1V" and "-1V" (c) voltage levels "2V" and "-2V"; (c) voltage levels "3V" and "-3V"

There are four switching configurations that are possible for output voltage level "0" [Table 3.1(a)], Three switching combinations are possible for output voltage levels "1V" and "-1V" [Table 3.1(b)], For output voltages "2V" and "–2V," there are two switching arrangements that are possible [Table 3.1(c)], There are one switching setups that are feasible for output voltages "3V" and "–3V" [Table 3.1(d)] .

Level of Output Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
3V	1	0	0	1	1	0	0	1
2V	1	1	0	0	1	0	0	1
1V	1	0	0	1	1	1	0	0
0	1	1	0	0	1	1	0	0
–1V	0	1	1	0	1	1	0	0
–2V	0	0	1	1	0	1	1	0
–3V	0	1	1	0	0	1	1	0

Table 3.2: Switching States for Seven Level

As shown in Table 3.2, a cascade of two H-bridges with a two-DC link ratio of 1:2 can produce seven levels of output voltage: 1V, 2V, 3V, 0, -1V, -2V, and -3V. In the case of 1:2 voltage source ratio, output voltage levels higher than seven levels cannot be produced.

By adjusting the DCLR, it is possible to modify the number of OVLs. The number of out voltage levels will increase to more than 7 if the DCLR is changed from 1:2 to 1:3. The source voltage will be different for 1:3, but the switch connection design will be the same as that in **Figure 3.1**. The ASHB MLI with a DCLR of 1:3 is depicted in **Figure 3.2**. The same switching configuration that is described in **Table 3.1** should be

used for the OVL "0". There are two switchable states for output voltages of 1V and –1V. For the OVLs of 2V and –2V, only one switching state is possible. According to equation (1), output voltage

$$V_{out} = V_{H1} + V_{H2}$$

The output voltage $V_{out} = 2V$ in this case only occurs when $V_{H1} = -1V$ and $V_{H2} = 3V$. Again, the output voltage is $V_{out} = -2V$ when $V_{H1} = 1V$ and $V_{H2} = 3V$.

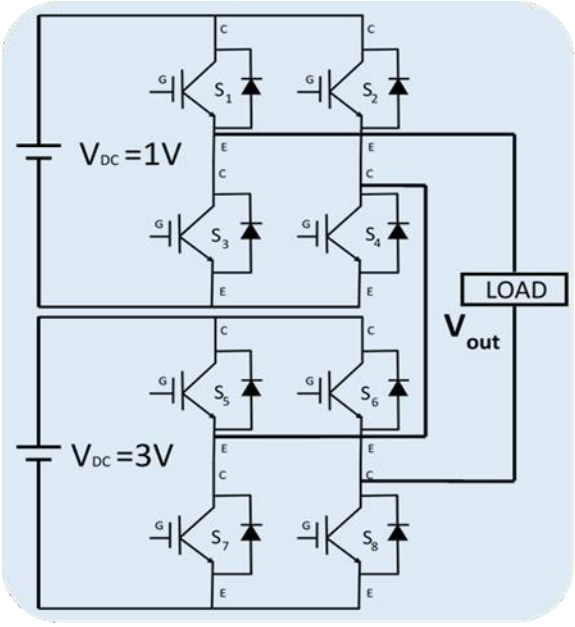


Figure 3.2: Cascading two HB with 1:3 DCLR

Level of voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1V	1	0	0	1	1	1	0	0
	1	0	0	1	0	0	1	1
–1V	0	1	1	0	1	1	0	0
	0	1	1	0	0	0	1	1

(a)

Level of voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
2V	0	1	1	0	1	0	0	1
–2V	1	0	0	1	1	0	0	1

(b)

Level of voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
3V	1	1	0	0	1	0	0	1
	0	0	1	1	1	0	0	1
–3V	1	1	0	0	0	1	1	0
	0	0	1	1	0	1	1	1

(c)

Level of voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
4V	1	0	0	1	1	0	0	1
–4V	0	1	1	0	0	1	1	0

(d)

Table 3.3: Switching configurations for: (a) OVLs "1V" and "-1V"; (b) OVLs "2V" and "-2V"; (c) OVLs "3V" and "-3V" (d) OVLs "4V" and "-4V"

Table 3.3(a) displays the switching state combination for output voltage 1V and –1V, and Table 3.3(b) provides the switching state combination for output voltage 2V and –2V. V_{H1} should be equal to 0 and V_{H2} should be +3V for an output voltage of 3V. Additionally, V_{H1} is equal to zero and V_{H2} is equal to –3V for output voltage of –3V, and for each OVL in this situation, two switching states are possible [Table 3.3(b)].

Level of Output Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
4V	1	0	0	1	1	0	0	1
3V	1	1	0	0	1	0	0	1
2V	0	1	1	0	1	0	0	1
1V	1	0	0	1	1	1	0	0
0	1	1	0	0	1	1	0	0
–1V	0	1	1	0	1	1	0	0
–2V	1	0	0	1	0	1	1	1
–3V	0	1	1	0	0	1	1	0
–4V	0	1	1	0	0	1	1	0

Table 3.4: Switching States for Nine Level

OVL 4V when V_{H1}=1V and V_{H2} =3V as well as output voltage –4V when V_{H1}= –1V and V_{H2}= –3V. The switching state combinations shown in **Tables 3.3 (d)**. Nine different voltage levels produced using DCLR 1:3. More than nine voltage levels cannot be achieved with this ratio. The total number of voltage levels is listed in **Table 3.4.**

V_{out} (in V)	V_{H1} (in V)	V_{H2} (in V)
0	0	0
1	+1	0
Voltage level 2V can't be achieved		
3	–1	+4
4	0	+4
5	+1	+4
–1	–1	0
–3	+1	–4
Voltage level -2V can't be achieved		
–4	0	–4
–5	–1	–4

Table 3.5: Switching States using DCLR 1:4

V_{out} (in V)	V_{H1} (in V)	V_{H2} (in V)
0	0	0
1	+1	0
Voltage level 2V can't be achieved. Voltage level 3V can't be achieved.		
4	–1	+5
5	0	+5
6	+1	+5
–1	–1	0
Voltage level -2V can't be achieved. Voltage level -3V can't be achieved .		
–4	+1	–5
–5	0	–5
–6	–1	–5

Table 3.6: Switching States using DCLR 1:5

It can generate nine distinct OVLs when utilizing DCLR of 1:4, although voltage levels of 2V and –2V are not achievable. **Table 3.5** displays the total OVLs using a 1:4 DCLR. The OVLs generated when using a 1:5 DCLR were the same nine, but it was impossible

to generate voltage levels of 2V, –2V, 3V, and –3V. The total OVLs that can be produced utilizing a 1:5 DCLR are shown in **Table 3.6**.

A maximum of nine OVLs can be produced and all voltage levels can be received at a 1:3 DCLR, it is confirmed in previous part, regardless of how two HBs are cascaded or what DCLR is used. Otherwise, some voltage levels will remain unattainable.

Case 02: Maximum OVLs with Cascading Three ASHB

This Case will cascade three HBs with three different voltage sources. The maximum number of OVLs and the three DCLR necessary to achieve the maximum number of OVLs will then be determined. The main goal of this paper is to determine the maximum number of voltage levels that can be obtained by cascading HBs, as well as the voltage source ratios needed to obtain the greatest number of levels possible without a voltage level gap.

To this end, when three DCLR are used, the voltage ratio of the first two HBs is fixed at 1:3, and the voltage ratio of the third HB must be changed because if two HBs are used, the maximum output voltage can be obtained at 1:3 DCLR, where any voltage level is not unachievable.

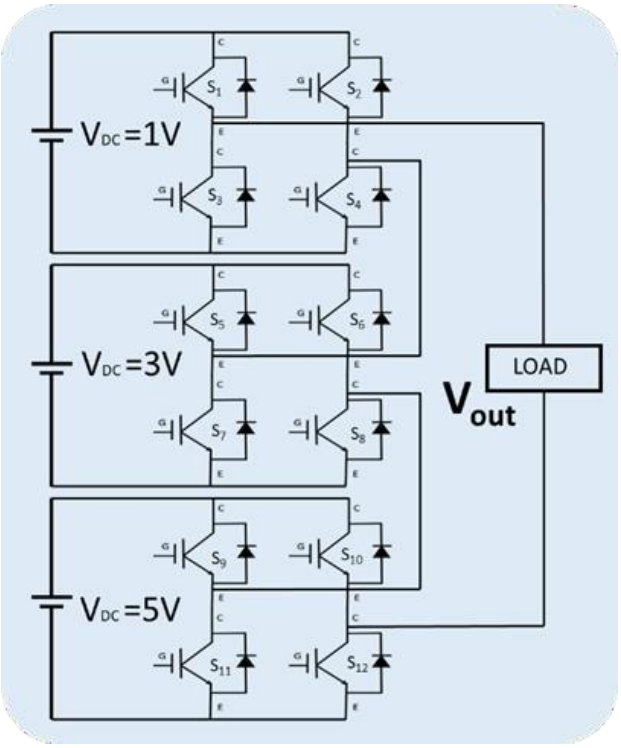


Figure 3.3: Cascading three HB with 1:3:5 DCLR

Along with three DC links, three HBs will be connected in series. The DCLR is 1:3:5 and it is being investigated how much OVLs these DCLR will produce. It was discussed in the previous section that a maximum of nine OVLs could be produced using two HBs.

V_{out} (in V)	V_{H1} (in V)	V_{H2} (in V)	V_{H3} (in V)
1	+1	0	0
2	–1	+3	0
3	0	+3	0
4	+1	+3	0
5	0	0	+5
6	+1	0	+5
7	–1	+3	+5
8	0	+3	+5
9	+1	+3	+5
0	0	0	0
–1	–1	0	0
–2	+1	–3	0
–3	0	–3	0
–4	–1	–3	0
–5	0	0	–5
–6	–1	0	–5
–7	+1	–3	–5
–8	0	–3	–5
–9	–1	–3	–5

Table 3.7: Switching States using DCLR 1:3:5

It should be necessary to increase the H bridge if you want to produce OVLs greater than nine. Three HB connections with a DCLR of 1:3:5 is shown in Figure 3.3

$$V_{out} = V_{H1} + V_{H2} + V_{H3} \quad (2)$$

The output voltage V is therefore the sum of each of the three HB output voltages, as deduced from equation (2). There are 19 different OVLs that can be produced by the ratio 1:3:5. **Table 3.7** depicts the conditions for the generation of the OVLs.

When using three HBs in cascading with different source voltages, the ratio will be fixed for the first two HBs while changing for the third HB. We can see that the maximum output voltages that 1:3:5 can produce are at the 19th level. The Third H Bridge voltage source ratio was changed from 5 to 9 [**Figure 3.4**] in order to increase the number of OVLs. The 1:3:9 ratio can then produce up to 27 different OVLs. **Table 3.8** shows the OVLs that can be generated by the DCLR of 1:3:9.

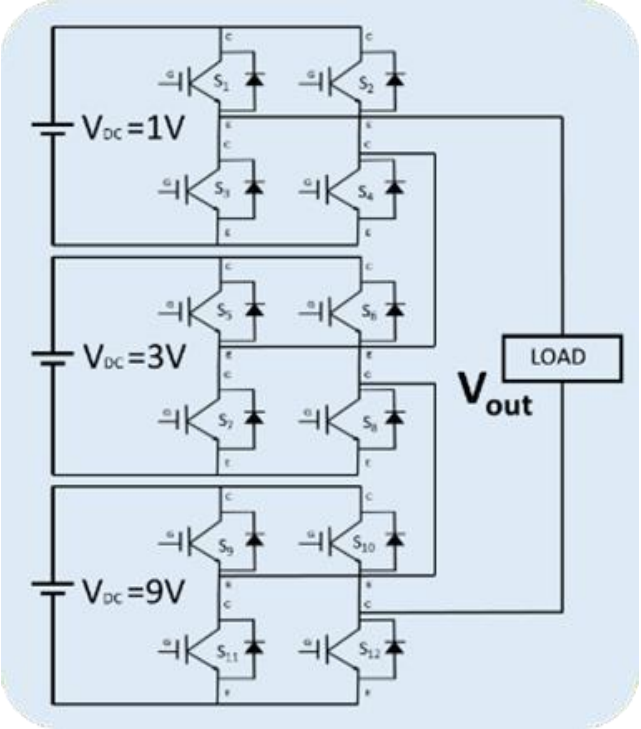


Figure 3.4: Cascading three HB with 1:3:9 DCLR

Here third H- bridge source ratio 10 is used. The third voltage ratio was supposed to be increased from 9 to 10 in order to raise the OVL above the 27 level. However, **Table 3.9** reveals that only 27th level can produce an output voltage where the - 5 and 5 voltage levels are indefinitely unreachable.

As a result, it can be said that the maximum number of OVLs, 27, can be created by cascading three HBs with a DCLR of 1:3:9 and that no voltage levels are impossible to achieve. It is not possible to increase the number of OVLs when the voltage ratio is increased beyond 1:3:9, and some voltage levels might continue to be unreachable.

V_{out} (in V)	V_{H1} (in V)	V_{H2} (in V)	V_{H3} (in V)
1	+1	0	0
2	–1	+3	0
3	0	+3	0
4	+1	+3	0
5	–1	–3	+9
6	0	–3	+9
7	+1	–3	+9
8	–1	0	+9
9	0	0	+9
10	+1	0	+9
11	–1	+3	+9
12	0	+3	+9
13	+1	+3	+9
0	0	0	0
–1	–1	0	0
–2	+1	–3	0
–3	0	–3	0
–4	–1	–3	0
–5	+1	+3	–9
–6	0	+3	–9
–7	–1	+3	–9
–8	+1	0	–9
–9	0	0	–9
–10	–1	0	–9
–11	+1	–3	–9
–12	0	–3	–9
–13	–1	–3	–9

Table 3.8: Switching States using DCLR 1:3:9

V_{out} (in V)	V_{H1} (in V)	V_{H2} (in V)	V_{H3} (in V)
1	+1	0	0
2	–1	+3	0
3	0	+3	0
4	+1	+3	0
Voltage level 5V is not achievable.			
6	–1	–3	+10
7	0	–3	+10
8	+1	–3	+10
9	–1	0	+10
10	0	0	+10
11	+1	0	+10
12	–1	+3	+10
13	0	+3	+10
14	+1	+3	+10
0	0	0	0
-1	–1	0	0

-2	–1	–3	0
-3	0	–3	0
-4	–1	–3	0
Voltage level –5V is not achievable.			
-6	+1	+3	–10
-7	0	+3	–10
-8	–1	+3	–10
-9	+1	0	–10
-10	0	0	–10
-11	–1	0	–10
-12	+1	–3	–10
-13	0	–3	–10
-14	–1	–3	–10

Table 3.9: Switching States using DCLR 1:3:10

Case 03: Maximum OVLs with Cascading Four ASHB

In Case 03, it is discussed that a maximum output voltage at the 27th level can be created by cascading three HBs. It will practice increasing the HB to raise OVLs. Therefore, four HBs will be cascaded in this section to determine the maximum OVLs that can be produced by doing so as well as the necessary DCLR for the greatest possible number of OVLs.

The voltage ratio for the first three HBs in a cascade of four HBs is fixed at 1:3:9. Because the 1:3:9 ratio will produce the most OVLs possible without a gap when cascading three HBs, the fourth voltage ratio will then be adjusted to determine the highest possible number of OVLs.

The maximum number of OVLs that can be produced by cascading four HBs is 81, and this is done without any gaps by using a DCLR of 1:3:9:27. In comparison to a number of 81, a number four HB voltage ratio below 27 will produce a lower OVL. Additionally, if the fourth voltage ratio is used above 27, it is impossible to achieve an OVL higher than the maximum output voltage of 81, and some voltage level gap will begin to form. Table 2.4 displays 81 OVLs produced by the 1:3:9:27 ratio.

The following sections discuss the generalized relationship found between voltage ratio and number of maximum OVLs from the discussion in the sections above as well as the generalized formula for the number of OVLs that can be generated from any voltage ratio.

3.3 Design Specifications for Output Voltage Levels

Section 01: Calculating the Number of Output Voltage Levels from Any Given DCLR

From the previous discussions, it is evident that cascading two HBs will produce output voltage at the ninth level. Next, the highest OVL was 27 when three HBs were cascaded. Following that, 81 OVLs can be produced using a cascade of 4 HBs. Therefore, in general, we can state that the maximum OVLs are

$$L_{max} = 3^N \tag{3}$$

when N is number of HBs with asymmetric voltage sources are cascaded.

Where L_{max} =maximum number of OVLs.

Now, if we look at the voltage ratio, we can see that 1:3 (for 9 levels), 1:3:9 (for 27 levels), and 1:3:9:27 (for 81 levels) voltage source ratios must be used in order to achieve the maximum number of OVLs without any level gaps. Therefore, the voltage source ratio we must use in order to cascade N number of HBs and obtain the maximum number of voltage levels without any voltage level gap is,

$$3^0 : 3^1 : 3^2 : 3^3 \ldots \ldots \ldots . : 3^N \tag{4}$$

It also called trinary ratio **[13]**. From the provided voltage ratios, the maximum number of OVLs can be calculated. If it tries, we should apply equation (5).

$$N_L = (S_r \times 2) + 1 \tag{5}$$

Where, $N_L = \text{Number of outputs volage levels}$

$S_r = \text{Sum of Voltage source ratios}$

Considering that the voltage ratio is 1:2:3:3, the OVLs that this voltage ratio can produce are

$$N_L = \{(1 + 2 + 3 + 3) \times 2\} + 1 \quad = 19$$

Therefore, it will produce 19 different OVLs using the voltage ratio 1:2:3:3 and cascading four HBs.

This equation allows the design of output voltage levels only with odd numbers. To design for the Nth level, ensure that N is an odd value. Additionally, the provided DCLR should be less than or equal to the DCLR associated with the maximum OVL without any gap.

Section 02: Calculating the Number of Output Voltage Levels from Any Given DCLR

Suppose, an ASHB MLI is to be designed that can generate 35 different OVLs. Therefore, we will determine the DCLR to be used when designing the 35th level AHSB MLI in this section, along with the amount of HB required.

Thus, the OVL indicated here is 35. Three asymmetric HBs can be cascaded to create a maximum of 27 different OVLs.

In addition, a maximum of 81 OVLs can be produced by cascading four asymmetric HBs.

Here, $27 < 35 < 81$

So, four ASHB need to be cascaded for 35 number of OVL.

We know from equation no,

$$N_L = (S_r \times 2) + 1$$

Here, $N_L = 35$

Therefore, $35 = \{(1 + 3 + 9 + x) \times 2\} + 1$

$35=26+2x+1$

$\therefore x=4$

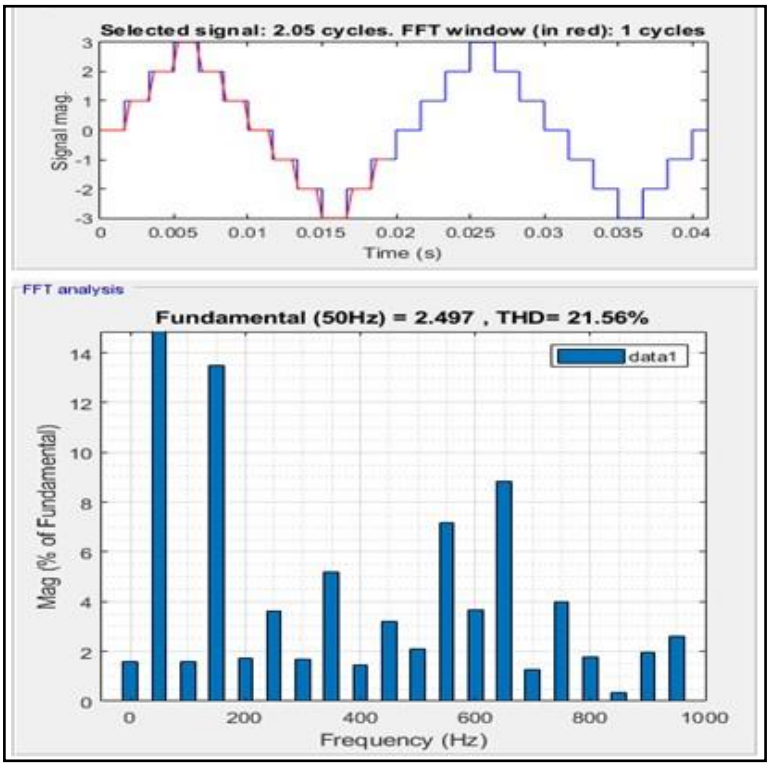
Unknown for 35 number of OVLs.

For a maximum of 27

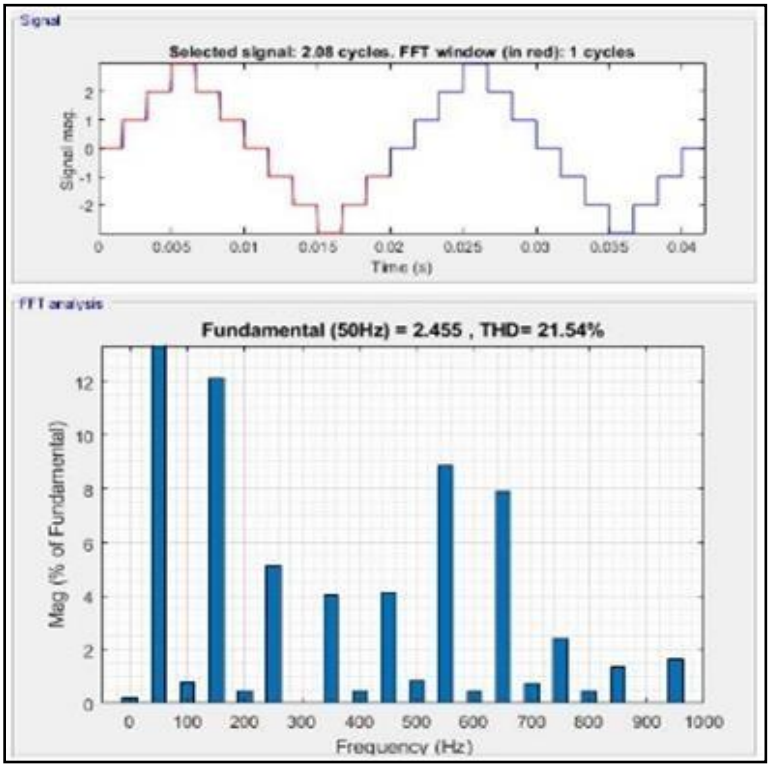
Therefore, four HBs must be cascaded and the DC links should be used in the ratio of 1:3:9:4 based on the OVL of 35.

3.4 THD Analysis for the Design System

Section 01: Maximum OVLs with Cascading Two ASHB

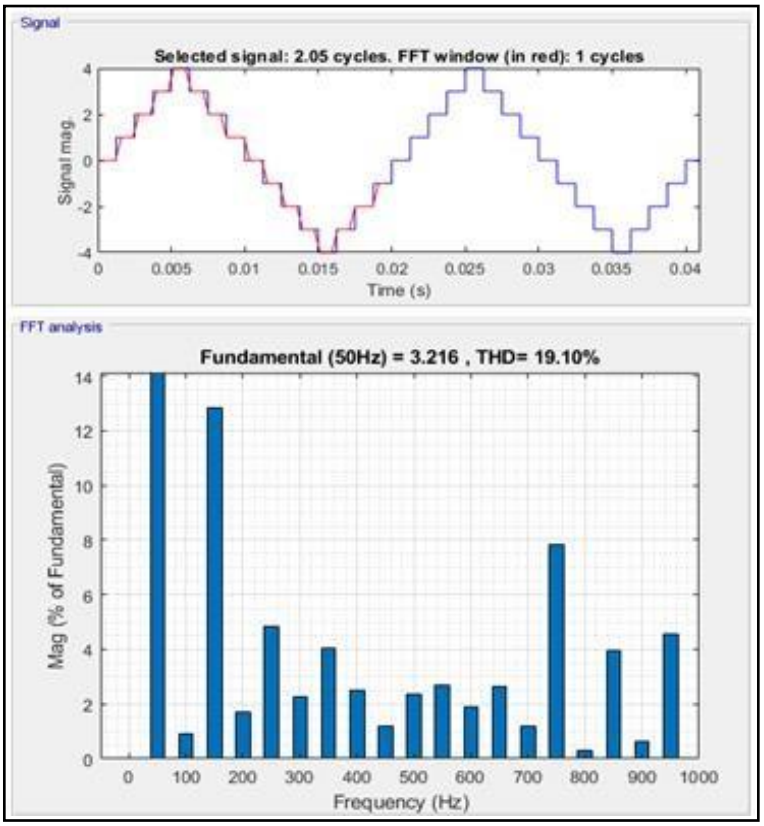


(a)

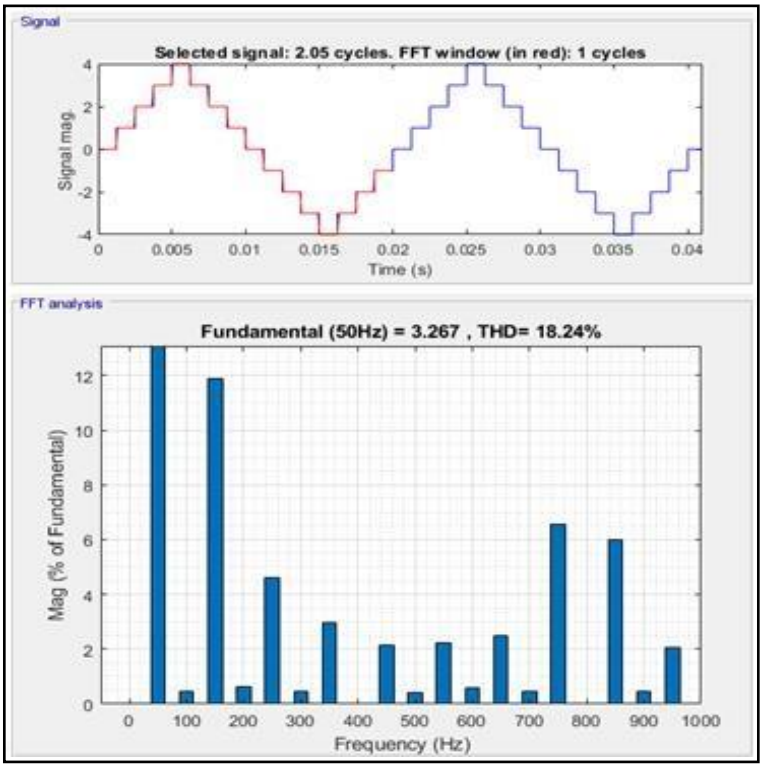


(b)

Figure 3.5: THD value of DCLR 1:2 when: (a) R load, (b) RL Load is used



(a)



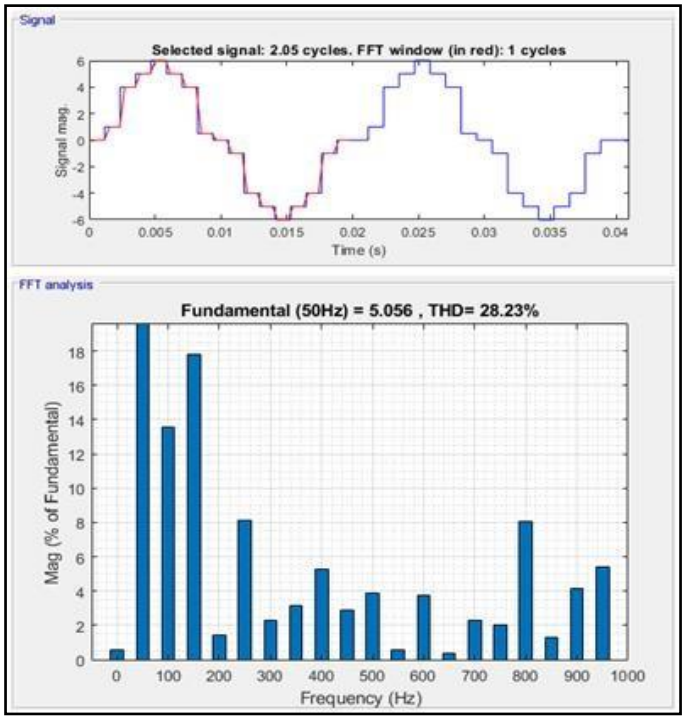
(b)

Figure 3.6: THD value of DCLR 1:3 when: (a) R load, (b) RL Load

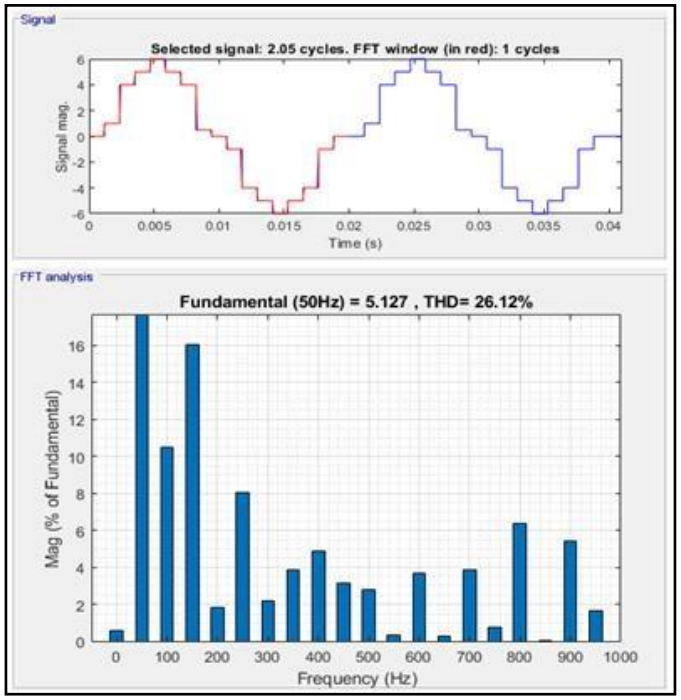
In Figure 3.5 and 3.6, the schematic diagrams depict two H-Bridge cascades featuring a 1:2 voltage ratio concerning resistive and inductive loads. Each cycle, represented in red, spans 0.02 seconds, while the blue color signifies two complete cycles, equivalent to 0.04 seconds. Notably, the fundamental frequency ratios for the resistive load (R load) and the inductive load with resistance (RL load) are 21.56% and 21.54%, respectively.

These illustrations offer a comprehensive visualization of the intricate interplay between voltage ratios, load types, and corresponding frequency characteristics within the H-Bridge cascades.

The voltage source ratio of the two H-bridges we employed was 1:3, and we calculated the overall harmonic distortion for both resistive and inductive loads. In the image, we show the 2.05 cycle (in blue), where the greatest fundamental frequency amplitude is 3.216 and the ratio of fundamental frequency (50 Hz) to the sum of its integer multiples of fundamental Frequency is approximately 19.10% for Figure 3.5 R load and 18.24% for Figure 1.6 R-L load. The fundamental frequency's maximum amplitude is 3.267. The red color in the image signifies one cycle. This may last 0.02 seconds. A total of nine Over voltage Levels (OVLs) can be generated, and these voltage levels are universally receivable through a 1:3 (DCLR) configuration, as conclusively established in the previous section.



(a)



(b)

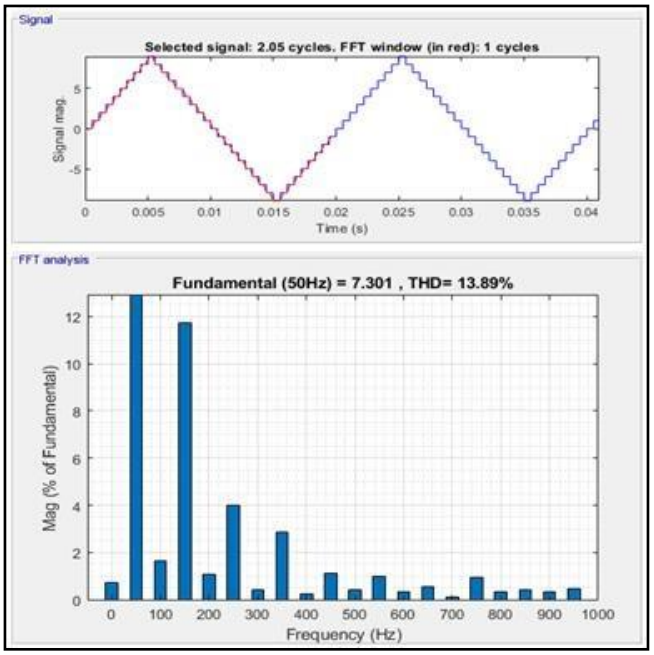
Figure 3.7: THD for Voltage Ratio 1:5: (a) R Load; (b) RL load

This holds irrespective of the specific manner in which two H-Bridges (HBs) are cascaded or the particular DCLR employed. The significance lies in ensuring that all voltage levels are accessible through this standardized 1:3 DCLR setup; otherwise, there exists the risk of certain voltage levels remaining unattainable, underscoring the critical role of the designated configuration

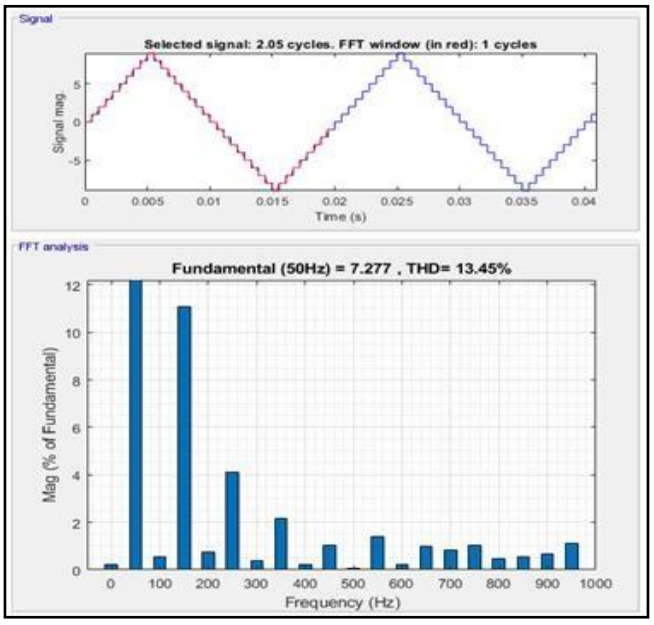
Total harmonic distortion for a 1:5 voltage ratio is shows in Figure 3.7 (a) & (b). where 2.05 cycle, which is depicted in blue, was captured. However, we have now selected the first cycle to do the Fast Fourier Transformation, which is shown by the color red. THD comparison will be larger than 1:3 voltage ratio since there is a level difference between 1V and 4V in this situation. Here, the ratio of the fundamental frequency and the total integer multiple of the fundamental frequency for the R load is 28.23%, which is 1.4780 times greater than the THD produced at 1:3 voltage ratio in Figure 3.7 and for the RL load, it is 26.12%, which means that the THD is 1.43201 times greater than the 1:3 voltage ratio.

Section 02: Maximum OVLs with Cascading Three ASHB

Here, we are figuring out the Total Harmonic Distortion for a 1:3:5 Voltage ratio. In Figure 3.8 and 3.9, When 2.05 cycles are present (in blue). The highest frequency up to 1000 HZ has been used in this case. The Fast Fourier Transform, which is shown in red and requires 0.02 seconds of the full wave, has now taken 1 cycle. Here, for the loads R and RL, the ratio between the fundamental frequency and the sum of the integer multiples of the fundamental frequency is 13.89%, whose amplitude is 7.301, and 13.45%, whose amplitude is 7.277.



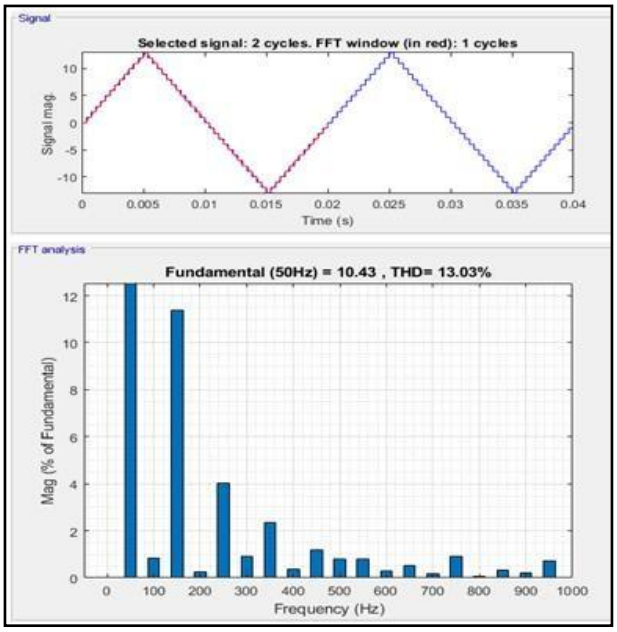
(a)



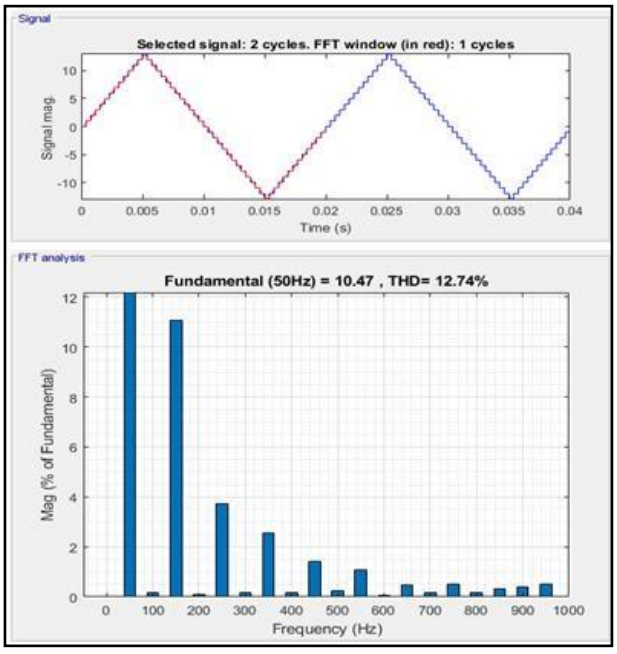
(b)

Figure 3.8: THD for Voltage Ratio 1:3:5: (a) R Load; (b) RL load

We previously estimated THD for a 1:3:5 voltage ratio. For a voltage ratio of 1:3:9, we compute Total Harmonic Distortion in Figures 3.8 and 3.9 Where 2.05 cycle, or 0.04 seconds, is calculated and shown in blue. But as indicated by the red hue, we have now chosen the first cycle to perform the Fast Fourier transformation. As there is no level gap in this situation, the THD ratio will be smaller than it would be for a 1:3:5 voltage ratio.



(a)



(b)

Figure 3.9: THD for Voltage Ratio 1:3:9: (a) R Load; (b) RL load

In this instance, the ratio of fundamental frequency and the sum of the integer multiple of fundamental frequency for R load is 28.23%, which is 1.066001 times smaller than the THD achieved in 1:3:5 voltage ratio, and 26.12% for R-L load, which is 1.055729 times less than the THD that was produced in 1:3:5 voltage ratio.

Section 03: Proposed THD Minimization Technique

Technique I: One of the two techniques for THD minimization is level jump, i.e. generating the next level without accepting one level. For example, we have an ASHB MLI that can generate ten levels. Those levels are 1V to 10V, incremented by 1V. It's THD is X%.

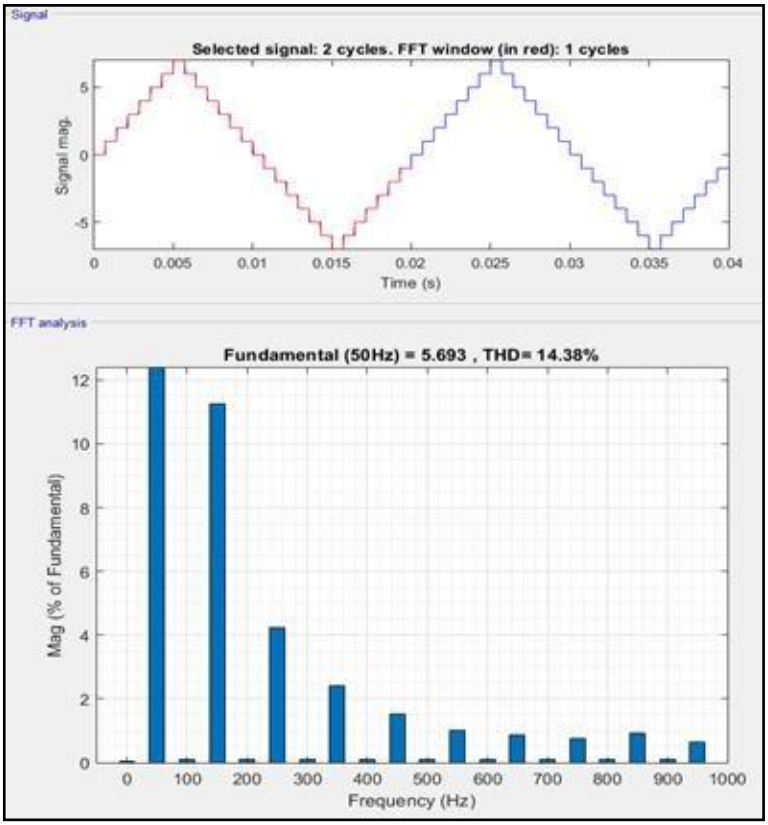
Now the ratio of this same MLI is selected in such a way that the level number at the output is ten bits without receiving the 5V level and generates 6V by level jump and the ten level is completed.

There is a total of fifteen levels generated, as shown in Figure 3.10(a), without any level jumps. It has a THD (R-L load) of 14.38% and a voltage ratio of 1:3:3 (three HB cascaded). Fig 3.10(b) illustrates how lowering THD by a level jump. The fifteen levels are generated here as well, but the level jumps to 4V without accepting the level after 1V. That is, a number of levels have been generated by the MLI without the 2V and 3V levels being accepted.

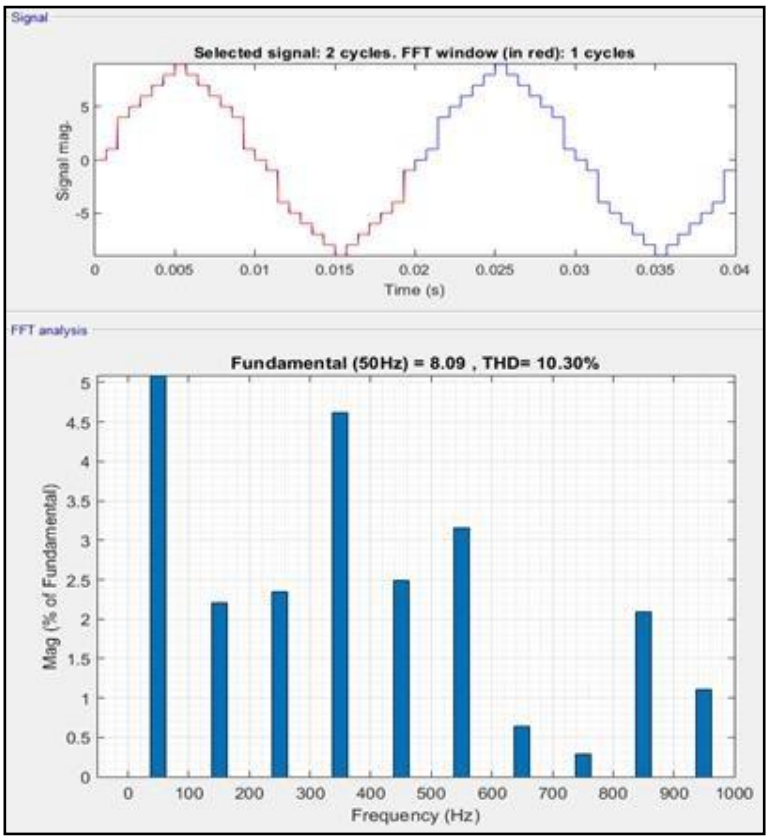
The THD of the 15 level ASHB MLI can be decreased through this level-jumping phenomenon from 14.38% to 10.30%, which is lower than the THD of the 27th level MLI [Fig 3.10(c)].

Normally, the switching state is not required to change when a level is jumped. The only way to choose a DC Link ratio properly is to allow for the proper level jump. Level jump requires careful consideration when choosing a ratio. THD will start to rise in the event of a level jump close to the peak level.

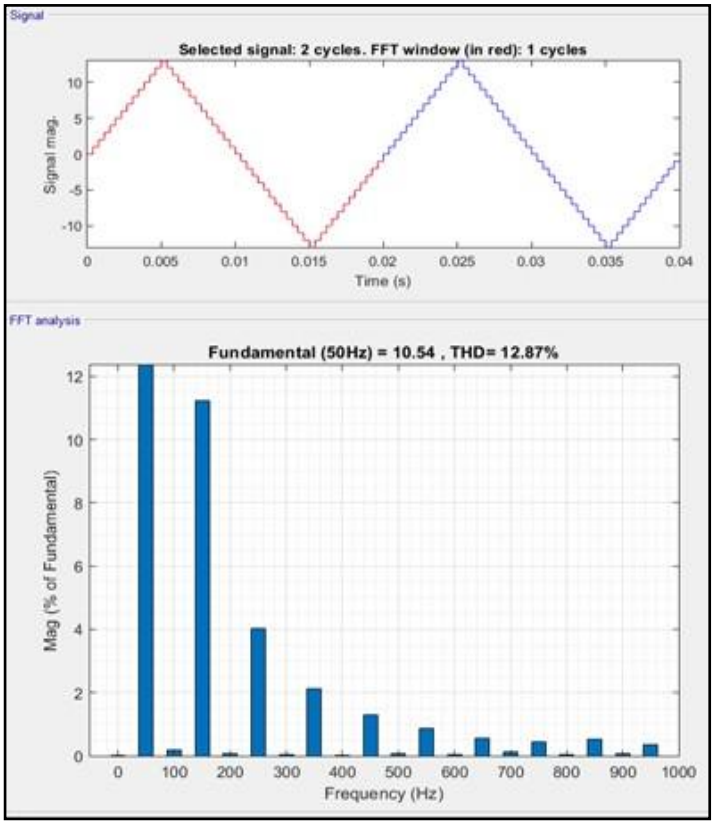
Technique II: The second technique is level repetition. By repeating the peak level or levels just below the peak level, the THD can be reduced. The output of a 15 level ASHB MLI is shown in Figure 3.10(d), where the THD is reduced to 6.52% by only repeating the peak level seven times. The switching state affects how many times this level is repeated. There are also restrictions at this repetition level. If the limit is exceeded, THD starts to rise once more.


Signal
Selected signal: 2 cycles. FFT window (in red): 1 cycles
Signal mag.
Time (s)
FFT analysis
Fundamental (50Hz) = 5.693 , THD= 14.38%
Mag (% of Fundamental)
Frequency (Hz)

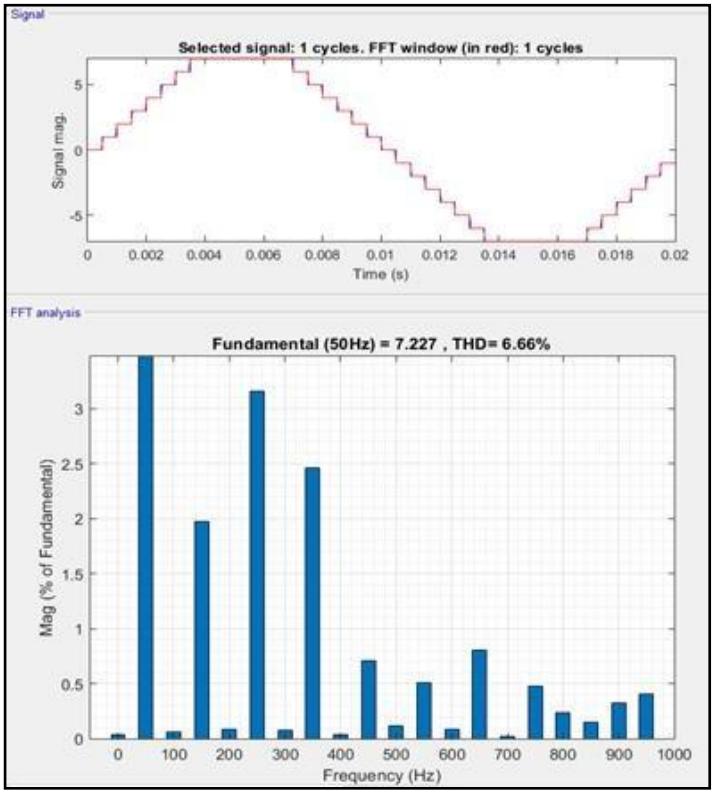
(a)


Signal
Selected signal: 2 cycles. FFT window (in red): 1 cycles
Signal mag.
Time (s)
FFT analysis
Fundamental (50Hz) = 8.09 , THD= 10.30%
Mag (% of Fundamental)
Frequency (Hz)

(b)



(c)



(d)

Figure 3.10: THD for: (a) fifteen levels without level jump; (b) fifteen levels with level jump; (c) 27th level MLI; (d) fifteen levels with level repetition.

3.5 Typical Design State Combining Techniques I & II

The discussion in the previous section demonstrated that THD can be decreased by a level jump or level repetition. Switching determines level repetition, and DC link ratio determines level jump. In this section, it is suggested that the ratio and switching of the 39-level ASHB MLI will reduce THD to 2.89% by combining the two techniques.

For the 39-level ASHB MLI design, we can use Equation (6). As we know, it is possible to design a maximum MLI of 27 levels by CASCADING three HB's and maximum 81 level inverter can be designed by caching four HB's.

Here, $N_L = 39$

Therefore, $39 = \{(1 + 3 + 9 + x) \times 2\} + 1$

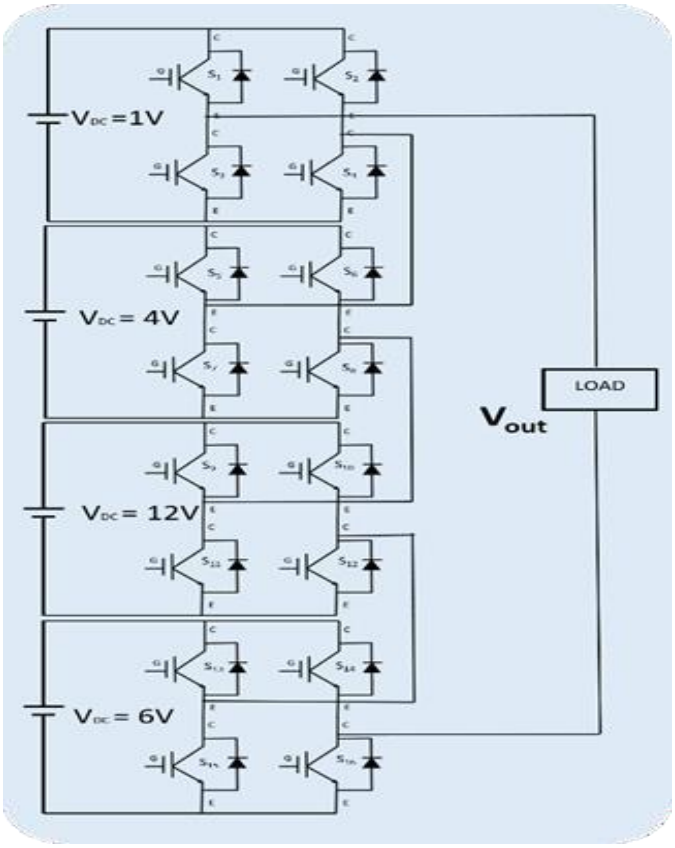
$$39 = 26 + 2x + 1$$

$$x = 6$$

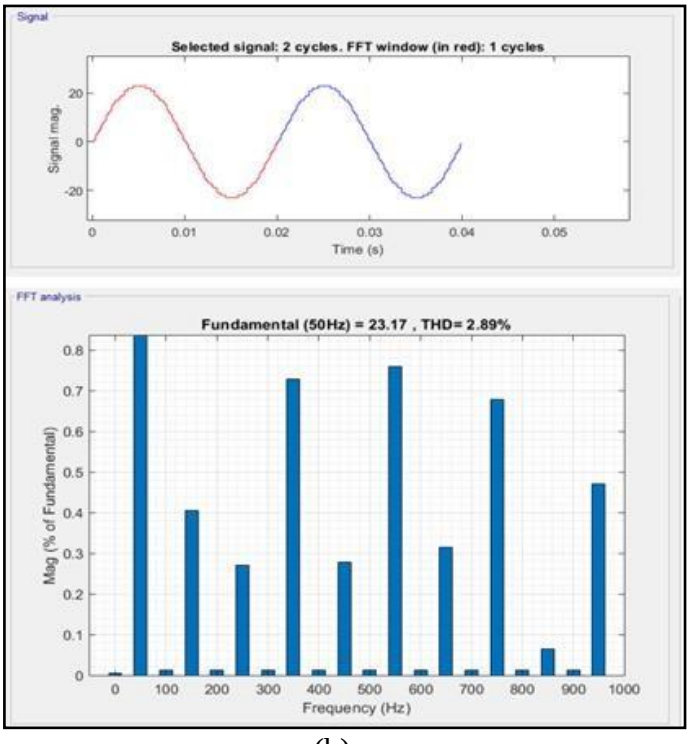
For a 39 level ASHB MLI design, the general ratio of four HBs is therefore 1:3:9:6. To lower THD to 2.89%, four H bridges in the ratio of 1:4:12:6 are proposed. There are some level repetitions through switching and some level jumps through ratio selection. The circuit diagram using the 1:4:12:6 ratio is shown in **Figure 3.11 (a)**. This ratio choice has resulted in level jumps occurring every two levels.

Instead of switching according to **Table 3.10**, 1:3:9:6 ratio switching can also be used. The only modification would be to repeat the peak level six times, the subsequent smaller level twice and the subsequent and subsequent smaller levels once. Then a THD of 2.89% will be produced by simply changing the ratio to 1:4:12:6 [**Figure 3.11 (b)**]. This ratio will generate 37 levels from 39 levels.

Moreover, the strategic selection of how levels are repeated and transitioned between allows for further enhancements in performance and precision within the system. This nuanced control over level repetition and transitions opens doors to refining the output quality and optimizing the operational efficiency beyond the conventional approaches stipulated in **Table 3.10.**



(a)



(b)

Figure 3.11: (a) Circuit Diagram using DCLR 1:4:12:6; (b) Value of THD when DCLR 1:4:12:6 is used

Number of levels	V_{out}	V_{H1}	V_{H2}	V_{H3}	V_{H3}
1	0	0	0	0	0
2	1	+1	0	0	0
3	3	–1	+4	0	0
4	4	0	+4	0	0
5	5	+1	+4	0	0
6	7	–1	–4	+12	0
7	8	0	–4	+12	0
8	9	+1	–4	+12	0
9	11	–1	0	+12	0
10	12	0	0	+12	0
11	13	+1	0	+12	0
12	15	–1	+4	+12	0
13	16	0	+4	+12	0
14	17	+1	+4	+12	0
	17	–1	0	+12	+6
15	18	0	0	+12	+6
16	19	+1	0	+12	+6
	19	+1	0	+12	+6
17	21	–1	+4	+12	+6
	21	–1	+4	+12	+6
18	22	0	+4	+12	+6
	22	0	+4	+12	+6
	22	0	+4	+12	+6
19	23	+1	+4	+12	+6
	23	+1	+4	+12	+6
	23	+1	+4	+12	+6
	23	+1	+4	+12	+6
	23	+1	+4	+12	+6
	23	+1	+4	+12	+6
	23	+1	+4	+12	+6
The same negative Voltage levels will be generated					

Table 3.10: Switching States using DCLR 1:4:12:6

3.6 Summary

In this chapter, we have explored three scenarios. In the first case, we examined a configuration involving two ASHBs, while the third case involved three ASHBs. The final case delved into the diagram, switching sequence, and Total Harmonic Distortion (THD) of three ASHBs. Throughout this discussion, we provided a specific design for a Multilevel Inverter (MLI). We introduced a formula that determines the number of levels achievable by incorporating the maximum number of H-Bridges. Using this formula, we devised a configuration with remarkably low THD. To further mitigate THD and align with IEEE standards, we implemented two specific techniques.

CHAPTER 4
RESULTS AND DISCUSSIONS

4.1 Observations

In the realm of Multilevel Inverter (MLI) design, prevailing practice involves using asymmetric DC voltage sources. This study introduces a fresh perspective, aiming to reveal the maximum attainable voltage levels with any quantity of asymmetric DC sources. We present a comprehensive equation to determine the full spectrum of voltage levels, applying it to design the Asymmetric Stacked H-Bridge (ASHB) MLI for diverse output voltage levels. Contrary to the common belief that increasing levels inherently reduces Total Harmonic Distortion (THD), we propose THD reduction through strategic level jumps and repetitions. By advocating for a specific voltage ratio within the ASHB MLI, we achieve substantial THD reduction. Additional techniques are employed to transform the output waveform towards a sinusoidal pattern, going beyond THD reduction to significantly reduce the required filter size at the converter's output. This not only improves overall efficiency but also potentially eliminates the need for extensive filtering. The combination of reparation and level jumping techniques shows promise for achieving a notable 1% THD reduction in the future, representing a significant advancement in MLI design and practical applications.

4.2 Discussions

This study delves into the exploration of asymmetric DC voltage sources within Multilevel Inverter (MLI) design, challenging conventional methods. The authors introduce a groundbreaking equation to unlock the maximum potential of voltage levels from asymmetric DC sources in the Asymmetric Stacked H-Bridge (ASHB) MLI, providing a practical dimension to theoretical frameworks. Contrary to common belief, the paper proposes a nuanced strategy involving deliberate level jumps and repetitions to reduce Total Harmonic Distortion (THD) rather than merely increasing levels. These strategies not only cut THD but also potentially reduce the required filter size, enhancing overall efficiency in MLI design. The study anticipates a 1% THD reduction, showcasing theoretical progress and practical promise for real-world MLI applications.

CHAPTER 5
PROJECT MANAGEMENT

5.1 Task, Schedule and Milestones

We select a topic and start the project on April 20, 2023. Gathering our resources took eight days. We have spent seven days conducting an in-depth analysis of the research paper. After that, we create simulation models and run them for 12 days. To get the investigation's output waveform with the THD value, we took eighteen days. We utilized 37 days to assess if THD is increasing or decreasing. We investigate THD reduction approaches for 37 days, of which 35 days are devoted to the proposal of two techniques. In order to implement the two techniques together in an MLI, we needed fourteen days. On November 1, 2023, we started drafting the report, and it took us 39 days to finish. Finally, on February 5, 2024, we filed our final report.

5.2 Resources

As resources, we use Google Scholar and MATLAB Simulink. We have collected or measured data using MATLAB Simulink, and we have looked for relevant research publications using Google Scholar. In addition, MATLAB Simulink is used to carry out our project.

5.3 Lesson Learned

We get an in-depth understanding of MLI and its applications. We also study the design of the controlling mechanism and control system of MLI. Additionally, we study how to create MLI in MATLAB Simulink for output waveform analysis.

CHAPTER 6

IMPACT ASSESSMENT OF THE PROJECT

6.1 Economical, Societal and Global Impact

This inverter has high conversion efficiency by reducing harmonics, so it minimizes power losses that occur due to the harmonics. This minimization of power loss is very effective for society because power losses are directly connected to energy losses. In addition, energy losses are very sensitive for society. For high conversion efficiency, this type of inverter creates a new better user experience in a practical application.

6.2 Environmental and Ethical Issues

Improvement of power quality is a big concern now days for increasing number of electronic loads. As an electrical engineer, we think that we can find some better solution to solve this issue. As discussed in the previous chapters, we have thoroughly worked on improvement of THD, which directly improvise the quality of the power to be delivered at the receiver's end. In addition, we need to mention that the inverters that we have designed here to achieve the target [as per the IEEE standard] reduces the use of filter circuits leads to a cost-effective and sustainable solution.

6.3 Utilization of Existing Standards or Codes

According to IEEE standards, when bus voltage $v \leq 1kv$, individual harmonics should be 5.0% and Total Harmonics should be 8.0%. In case of bus voltage $1kV < v \leq 69kV$, Individual harmonics should be 3.0% and Total Harmonics should be 5.0%. Our proposed inverter fulfills this standard.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

The research being conducted analyzes the Asymmetrical H-Bridge Multilevel Inverter as an economically sustainable alternative for applications requiring large amounts of power. It provides superior waveforms with considerably lower Total Harmonic Distortion because of its novel structure and effective voltage level generation. To customize inverters to meet particular applications, the proposed equation to produce the N^{th} level of the ASHB MLI provides useful suggestions. Along with that, we introduce an approach that additionally minimizes total harmonic distortion (THD), which ultimately results in an output waveform that is similar to a sinusoidal wave. Thus, the converter has output filter size may be substantially decreased or eliminated, enhancing overall efficiency. By integrating reparation and level jumping, it can be achieved to achieve an impressive 1% reduction of total harmonic distortion (THD) in future periods.

7.2 New Skills and Experiences Learned

Succeeding in the design of a Nth level inverter employing an asymmetric H-bridge MLI topology and methods to reduce Total Harmonic Distortion (THD) allows possibilities to develop expertise in simulation, troubleshooting, power electronics design, and the practical implementation of multilevel inverters. By gaining such understanding, we will be more effective in designing circuits, choosing components, modulation methods, filtering techniques, control strategies, and optimization. This will assist us in making superior power electronics systems and sustainable power technologies.

7.3 Future Recommendations

High Voltage DC Transmission: Maximizing the number of levels for a particular power circuit configuration can improve the performance of an Asymmetrical H-Bridge Multilevel Inverter in high-voltage DC transmission. Adopting cascaded H-bridges topology and using asymmetrical input voltages can increase the number of levels.

Flexible AC Transmission System (FACTS): The performance of multilevel inverters can be improved by reducing the number of power-electronic switches, which

leads to a significant amount of energy being lost as a cause of high-frequency switching. A modified single-phase inverter, a development of a conventional H-bridge structure, can generate 15 levels of single-phase voltage output. Selective Harmonic Elimination can be employed to eliminate the lowest-order significant harmonics.

High-voltage and Medium-voltage Motor Drives: Asymmetric cascaded H-bridge topologies with unequal input DC voltages with different devices in various parts of the cascaded H-bridge inverter represent significant improvements in medium-voltage industrial drives. The proposed modulation technique blends the advantages of multi-carrier pulse width modulation and staircase modulation to improve the THD and reduce the switching losses over a wide range of modulation indexes.

Utility Interface for Renewable Energy: Multilevel inverters emerged as the solution for overcoming the limitations of two-level inverters, such as total harmonic distortion, high magnetic interference, and high $\frac{dv}{dt}$ in high power voltage applications. The ability to generate sinusoidal output voltage is another specialty of multilevel inverters. The performance improvement of multilevel inverters has attracted the attention of researchers.

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APPENDIX A

TURNITIN REPORT

ORIGINALITY REPORT

22%	20%	14%	11%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	dspace.daffodilvarsity.edu.bd:8080 Internet Source	5%
2	www.researchgate.net Internet Source	1%
3	www.ijrer-net.ijrer.org Internet Source	1%
4	Submitted to Higher Education Commission Pakistan Student Paper	<1%
5	Salman Ahmad, Atif Iqbal, Mohammad Ali, Khaliqur Rahman, Abdellahi Sidi Ahmed. "A Fast convergent Homotopy Perturbation Method for Solving Selective Harmonics Elimination PWM Problem in Multi Level Inverter", IEEE Access, 2021 Publication	<1%
6	researchid.co Internet Source	<1%
7	www.ijireeice.com Internet Source	<1%

APPENDIX B

COMPLEX ENGINEERING PROBLEM SOLVING AND ENGINEERING ACTIVITIES

Complex Engineering Problems (P) Solving		
	Attributes	Statement from students
P1	Depth of knowledge required	Improving the quality of power without low harmonics is the dominant topic in the power sector. The next world will depend on renewable energy sources, and harmonics will be the main problem in this way of power generation. To mitigate this problem of the modern era, we mainly focus on how to solve it reliably. Our thesis is mainly focused on asymmetric H-bridge MLI with low THD, and our thesis is a testament to the depth of the knowledge we have acquired to explore this avenue. Our comprehensive study mainly extends to the Nth-level asymmetric MLI, mitigating total harmonic distortion at a very low level and providing good power generation quality. We harnessed data on THD and level count and switched uses from the existing Google Scholar research papers to demonstrate the viability of electricity generation with low harmonic distortion and the best power quality.
P2	Range of conflicting requirements	❖ Several issues, including maintenance expenses, dependability, initial cost, and public awareness, come up whenever a project is undertaken in response to public demand. Small-scale H-bridge multilevel inverters are utilized for both small-scale residential applications and small-scale renewable energy power grids. On the other hand, it will be cost-effective because of its low startup and ongoing costs. When they choose a cost-effective solution, which limits the amount of power produced. ❖ However, to guarantee long-term reliability, it is beneficial to select a large-scale grid system MLI and Low THD with the best performance record. Everyone will adapt our hardware implementation to fit their unique circumstances once we demonstrate its extraordinary influence on the inverter and renewable energy sectors. Asymmetric H-bridge MLI architecture on a large scale with low THD may affect the nation's power system.
P3	Depth of analysis required	Comprehensive analysis is needed for research on multilevel inverters with THD in several areas, including simulation, environmental impact, and

		system design. The research objectives will figure out the level of analysis required however to get significant results, a thorough approach is frequently required.
P4	Familiarity of issues	Unlike the traditional MLI topology, our research has primarily focused on ways to minimize the THD and increase power quality. We found that the majority of them are frequently connected to traditional MLI topology in the power industry after conducting an online survey. Our new MLI topology reduces the primary issue facing the power sector when viewed through a perspective of renewable energy or the inverter industry. Our new MLI topology has a novel impact on the field of renewable energy.
P5	Extent of applicable codes	We strictly followed the regulatory framework established and approved by the Government of Bangladesh and the Institute of Electrical and Electronics Engineers (IEEE). Throughout this research, we exhibit a commitment to alignment with these codes and standards. Through simulation, we must follow the IEEE standards when reducing the total harmonic distortion of the symmetrical H bridge multilevel inverter. We have also ensured that our work strictly follows the Electricity Grid Code 2019 (Section 17.2.4) guidelines of the Bangladesh Energy Regulatory Commission (BERC) as well as the Institution of Electrical and Electronics Engineers (IEEE).
P6	Extent of stakeholder involvement and conflicting requirements	Our research project involved stakeholder involvement and conflicting requirements through direct survey forms, which enabled us to gain a comprehensive understanding. These surveys were crucial for assessing awareness and soliciting feedback from stakeholders. In order to determine the sort of harm that a rise in THD does to the home load, we have gathered data from several categories of electrical users. Furthermore, in order to construct a solar home system using our MLI, one must adhere to the requirements set out by the Sustainable and Renewable Energy Development Authority (SREDA).
P7	Interdependence	An important consideration in energy audits is total harmonic distortion. An electrical motor's effective time reduces with an increase in total harmonic distortion. We hope to demonstrate through this research how to reduce total harmonic distortion and prevent damage to our equipment. Energy auditing and approaches for minimizing total harmonic distortion are interconnected in this case.

Complex Engineering Problems (P) Solving		
	Attributes	Statement from students
A1	Range of resources	Developing a high-level inverter with asymmetric H-Bridge MLI structures along with utilizing techniques to minimize Total Harmonic Distortion (THD) can be achieved through the utilization of various resources. These resources include IEEE 519-2022 for THD, software for modeling like MATLAB Simulink, and research articles. Through the implementation of advanced techniques like pulse width modulation (PWM) and selective harmonic elimination (SHE) methods, the presence of harmonics in the output signal can be substantially minimized. This leads to a smoother and more efficient power conversion technique.
A2	Level of interaction	Our renewable energy industry is enhanced by the Asymmetric H-Bridge Multilevel Inverter, which may be used in wind and solar farms. We can use electric vehicles to make a contribution to the automotive industry. Our study has been extensively involved in the crucial process of assessing and collaborating with these resources in order to identify the most appropriate and viable option for Bangladesh's future energy environment.
A3	Innovation	We primarily give a generalized form in this research by examining various Asymmetrical H-bridge multilevel Inverter instances. We can determine the number of levels in any voltage ratio using this. To further enhance our system's power quality, we additionally suggest two methods for lowering Total Harmonic Distortion (THD).
A4	Consequences of society and environment	Our implementation work on the Nth Level Inverter, which utilizes an Asymmetric H-Bridge MLI Topology along with techniques to minimize Total Harmonic Distortion (THD), can have significant effects on society and the environment. It may substantially reduce energy waste and enhance the quality of power. This is aligned with sustainability objectives, encourages the development of cleaner energy infrastructure, and reduces environmental effects. Enhancing power quality has the further benefit of improving the reliability of the electrical system, leading to response improvement in sectors such as industry,

		and transportation, and contributing to advancement in both society and the economy.
A5	Familiarity	It is common in power electronics to use the Nth level inverter, which has an asymmetric H-bridge MLI structure, because it can generate superior output voltage waveforms and use advanced modulation techniques to reduce total harmonic distortion (THD). In motor drives, uninterruptible power supply, and renewable energy systems, it is broadly utilized.

APPENDIX C

SIMULINK DIAGRAM

Case 01: Maximum OVLs with Cascading Two ASHB

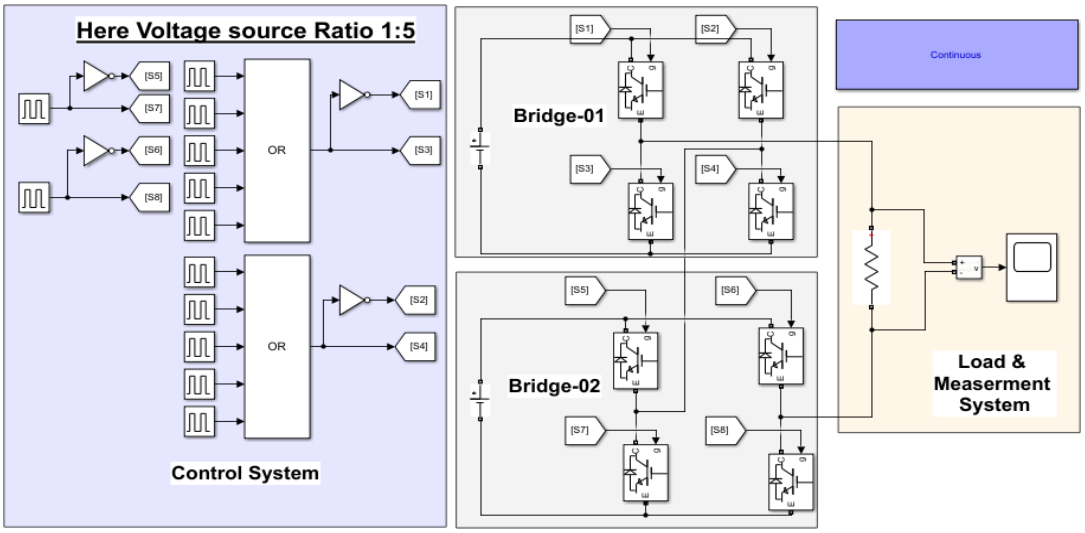

Figure 4.1: Simulation diagram for Two ASHB

Case 02: Maximum OVLs with Cascading Three ASHB

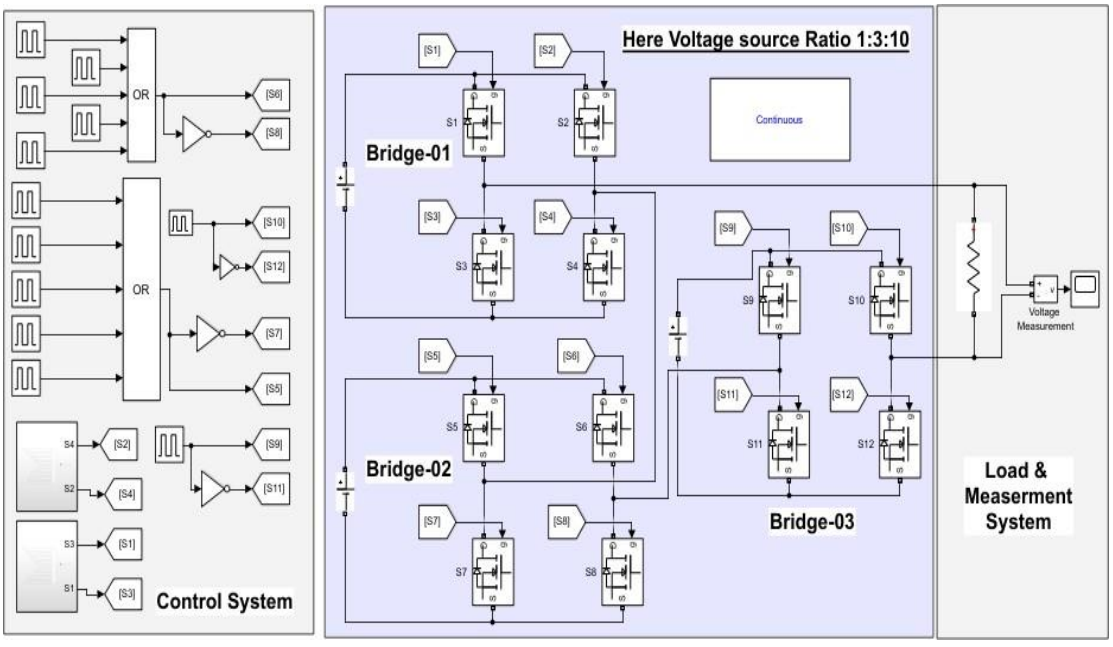

Figure 4.2: Simulation diagram for Three ASHB

Section 03: Proposed THD Minimization Technique

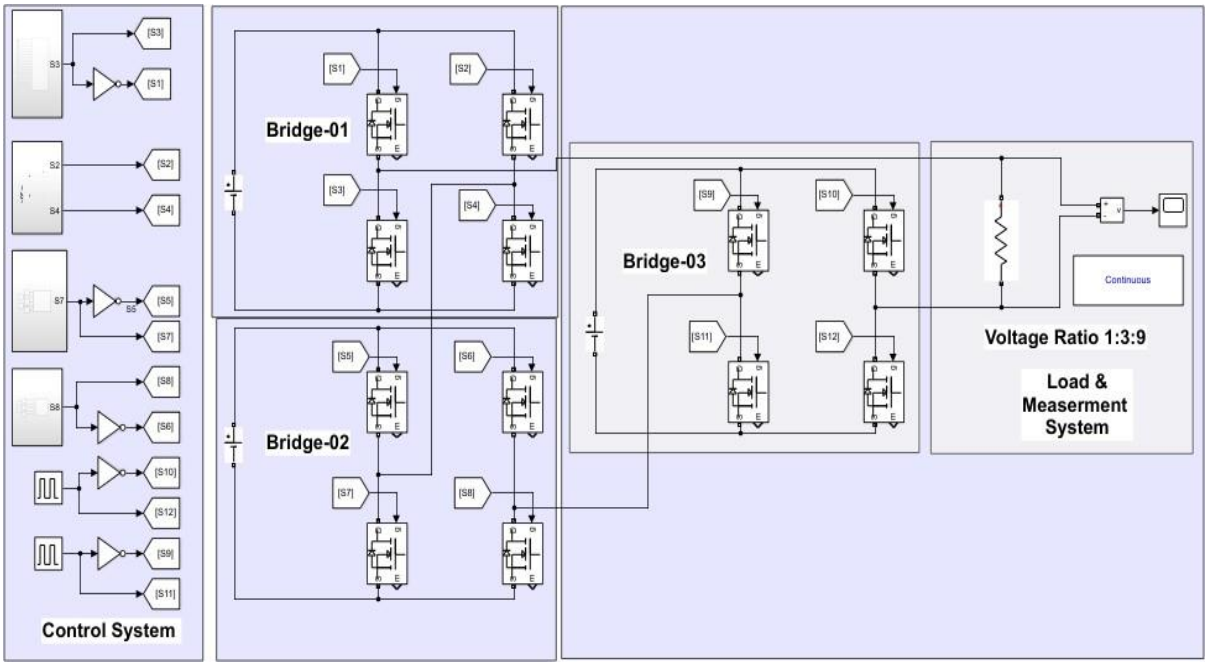

Figure 4.3: Simulation Diagram for Techniques I

Typical Design State Combining Techniques I & II

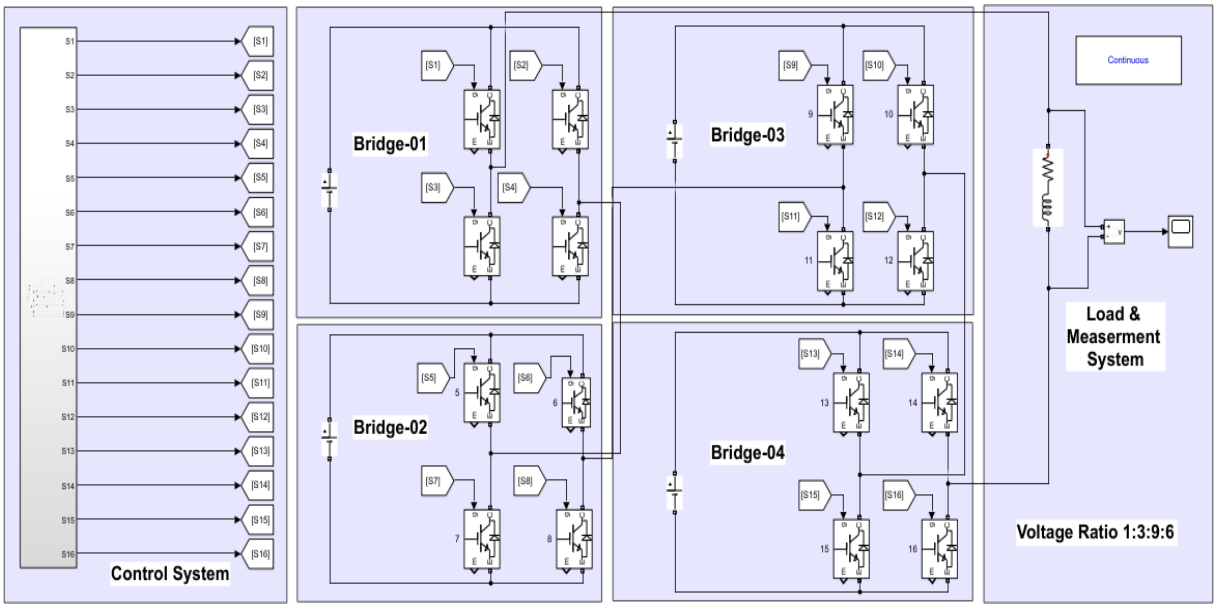

Figure 4.4: Simulation Diagram for Techniques I & II