NUMERICAL INVESTIGESTION OF NANOWIRE GaAs/InN GATE-ALL-AROUND TFET WITH $HfO_2/TiO_2/HfO_2/BaTiO_3$ GATE STRUCTURE

A Thesis paper is submitted in partial fulfillment of the requirements for the award of Degree of Bachelor of Science in Electrical and Electronic Engineering.

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FEBRUARY, 2023

DECLARATION

I hereby declare that this project **"NUMERICAL INVESTIGESTION OF NANOWIRE GaAs/InN GATE-ALL-AROUND TFET WITH $HfO_2/TiO_2/HfO_2/BaTiO_3$ GATE STRUCTURE**" represents my own work which has been done in the laboratories of the Department of Electrical and Electronic Engineering under the Faculty of Engineering of Daffodil International University in partial fulfillment of the requirements for the degree of Bachelor of Science in Electrical and Electronic Engineering and has not been previously included in a thesis or dissertation submitted to this or any other institution for a degree, diploma or other qualifications. I have attempted to identify all the risks related to this research that may arise in conducting this research, obtained the relevant ethical and/or safety approval (where applicable), and acknowledged my obligations and the rights of the participants.

Signature of the candidates

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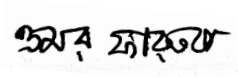

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APPROVAL

The project entitled **"NUMERICAL INVESTIGESTION OF NANOWIRE GaAs/InN GATE-ALL-AROUND TFET WITH $HfO_2/TiO_2/HfO_2/BaTiO_3$ GATE STRUCTURE"** submitted by **Md. Mehedi Hassan ID: 191-33-5017 & Md. Omar Faruqe ID: 191-33-4931** has been done under my supervision and accepted as satisfactory in partial fulfillment of the requirements for the degree of **Bachelor of Science in Electrical and Electronic Engineering** in **February, 2023.**

Signed

05.03.2023

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Dedicated
To
Our parents and teachers.
For their endless love, support and encouragement.

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LIST OF ABBREVIATIONS

FET	Field-effect transistor
GAA-FET	Gate-All-Around FET
BTBT	Band to band tunneling
DIBL	Drain-induced barrier lowering
TFET	Tunnel Field Effect Transistor
MOSFET	Metal oxide semiconductor field-effect transistor
SCE	Short channel effect
FeFET	Ferroelectric field-effect transistor
TCAD	Technology computer-aided design

LIST OF SYMBOLS

Symbol	Name of the symbol
Φ	Phi
Ψ	Psi
ρ	Rho
μ	Mu, Mobility
γ	Gamma

ACKNOWLEDGEMENT

First of all, we want to give thanks to **Almighty Allah**. With his blessing we are able to complete our work with best effort.

We want to pay our utmost respect to our Supervisor **Asif Hassan, Lecturer** of the **Department of EEE, Daffodil International University** for who has given us the chance to work on an impactful idea and taken care of every issue of development of this concept. Then we would like to take this opportunity to express gratitude to our supervisor for being dedicated in supporting, motivating and guiding us throughout this project. This project can't be done without his useful advice and help. Also thank him very much for giving us the opportunity to work with this project.

We also want to convey our thankfulness to **Md. Dara Abdus Satter, Associate professor & Associate Head** of the **Department of EEE, Daffodil International University** for his support and encouragement. Apart from that, we would like to thank our entire class fellows for sharing knowledge; information and helping us in making this project a success. To beloved family, we want to give them our deepest love and gratitude for being very supportive and also for their inspiration and encouragement during our studies in this Institution.

ABSTRACT

Using TCAD simulation, we demonstrated a nanowire gate-all-around (GAA) tunnel field-effect transistor (TFET) based on the GaAs/InN heterostructure. In the gate stacking, we proposed a tri-layer HfO2/TiO2/HfO2 high-K dielectric and a ferroelectric (FE) layer of barium titanate (BaTiO3). Because of its improved electrostatic control and quantum mechanical tunneling, the proposed GAA-TFET overcomes the thermionic limitation (60 mV/decade) of conventional MOSFETs' subthreshold swing (SS). Simultaneously, the state of ferroelectric materials improves TFET performance by exploiting differential amplification of the gate voltage under certain conditions. The very low DIBL of 13 mV and the transconductance of 4.92 mS are the most surprising discoveries of this device, which outperforms all previous results. The 5 nm barium titanite results in the lowest SS of 55 mV/dec. Furthermore, the output characteristics revealed a significant on-state current of 27.5A, and I_{ON}/ I_{OFF} ratio of 1.831 x 109, and a threshold voltage of 0.95. As a result, all the results suggest that the proposed device structure may pave the way for a new path for electronic devices, resulting in higher speed and lower power consumption.

Keywords- BTBT, gate-all-around structure, heterojunction, nanowire tunnel-FET.

CHAPTER 1
INTRODUCTION

1.1 Introduction

MOSFETs are subject to a number of performance limitations as integrated circuit technology advances towards the nanoscale, including short channel effects, high leakage current, a sub - threshold swing limit of 60 mV/dec, and others. In place of MOSFET, Tunnel Field Effect Transistor (TFET) is employed as an alternative device structure to address these shortcomings. Little sub threshold swing and low leakage current are features of TFET devices [1][2][3]. For ultra-low power applications, it has a low operating voltage and reduces short channel effects (SCEs) to a larger extent [4][5][6]. Although a TFET is seen to be a good fit for CMOS technology, it has some drawbacks such ambipolar behavior and a low ON current. The limits of TFETs have been the subject of numerous research projects. The direct band gap and better carrier mobility of III-V semiconductor material-based devices make them the preferable choice [7].

There has been a surge in demand for high-speed, low-power electronics in recent years. New transistor technologies have been critical in meeting this demand. The GaAs/InN GAA-FET transistor technology is a promising transistor technology that has gained popularity due to its high performance while consuming little power. A cylindrical gate surrounds the channel in GaAs/InN GAA-FETs, providing better control over current flow. Speed, power consumption, and scalability are all improved by this design.

Ferroelectric accoutrements can be used as a gate insulator in GaAs- grounded field-effect transistors (GaAs FETs). This type of device is known as a ferroelectric-gate FET (FeFET) or a ferroelectric field-effect transistor (FeFET). In a FeFET, the gate insulator is made of a ferroelectric material such as the material we use for this thesis barium titanate ($BaTiO_3$). The ability of an electric field to control the robotic polarization of these accoutrements is unique.

When you apply a voltage to the gate, the polarization of the ferroelectric material changes, affecting the electric field in the channel and the device's conductivity. FeFETs outperform traditional FETs in a variety of ways, including lower power consumption, faster speed, and non-volatility. They are being investigated [8].

1.2 Research Background

The concept of negative capacitance of FE materials in the gate stack of TFETs has recently been presented as extremely advantageous for energy band bending due to internal voltage amplification that increases the BTBT probability [9][10]. The NC effect in FE materials amplifies the difference in surface potential (ψs) in field-effect transistors, as shown in Fig 1.1 in relation to the gate voltage ($\frac{\partial V_g}{\partial \psi_s}$) transition. Salahuddin and Datta [11] demonstrated theoretically that a ferroelectric insulator operating in the negative capacitance region could act as a step-up transformer, resulting in several changes in the TFET configurations of SS, I_{ON}, and I_{OFF}, providing a new promising alternative without changing the fundamental physics of the FET. Sub-threshold swing (SS) is defined as follows:

$$SS = \left[\frac{\partial\, log_{10}(I_d)}{\partial V_g}\right]^{-1} = \underbrace{\left[1 + \frac{C_s}{C_{ox}}\right]}_{\text{Body Factor}} \underbrace{\left[\frac{\partial \psi_s}{\partial\, log_{10}(I_d)}\right]}_{\text{Transport Factor}}$$

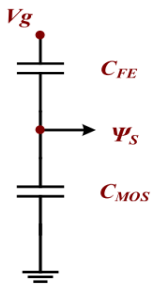


Fig.1.1: The equivalent capacitance scheme.

where Vg is the gate potential, Id is the drain to source current, and Cox and Cs are the gate oxide and semiconductor capacitors, respectively.

When a negative value of Cox is provided (indicating that FE is in the NC region), the equivalent capacitance is greater than Cs and the gate's combined capacitance is increased, resulting in a lower voltage being required to generate the same amount of charge Q. This results in the body factor<1, which lowers the SS while increasing the steep slope region. As a result, NC can assist TFETs in achieving a sharp OFF-to-ON transition and an appropriate I_{ON} /I_{OFF} value. For example, Kobayashi et al. discover an on-current of 15 A and an I_{ON}/I_{OFF} of 10^7, where it suppresses the mentioned earlier results [12]. Saeidi et al. experiment with a lower SS value of 15 mV/dec and a relatively high transconductance (gm) value of 3 mS to emphasize negative capacitance in TFET. Even though numerous studies on NCTFETs have been conducted, a relatively new device structure or physics is required to improve results much further [13][14].

1.3 Motivation

We introduced a nanowire-GAA structure in this paper to enhance TFET performance. Using TCAD simulation, we suggested and evaluated a GaAs/InN heterostructure-based nanowire gate-all-around tunnel FET (GAA-TFET). We demonstrated the GaAs/InN heterostructure by taking several key properties of both GaAs and InN into account, including effective mass, narrow optical band gap, high saturation velocity, and high mobility, all of which are very congruent for validating an excellent TFET [15]. In addition, InN growth on a GaAs substrate [16] and fabrication of GaAs/InN heterostructure-based photovoltaic cells [15] have recently been accomplished. Internal InN channel polarization generates an uncompensated sheet charge at the GaAs/InN heterointerface, which can be used to generate significant internal electric fields and Interband tunneling. Furthermore, the piezoelectric properties of these materials, in conjunction with the lattice mismatch, contribute to an additional polarization discontinuity [17][18].

In the proposed structure, a tri-layer HfO2/TiO2/HfO2 high K-dielectric was used as the gate insulating oxide, and a $BaTiO_3$ ferroelectric material was used. The $BaTiO_3$ had a significant impact on the GAA-TFET, with an on-state current of 27.5uA, an I_{ON}/I_{OFF} ratio of 1.831×10^9, and a transconductance of 4.92 mS. Furthermore, the SS drops dramatically, with the lowest SS measured at 55 mV/dec and a threshold voltage of 0.95V. The proposed device's outstanding findings add another dimension to the never-ending quest for better performance of nano-electronic devices.

1.4 Objectives

The following are the main goals of this thesis:

1)By modifying the gate geometry in conjunction with the impact of FE, we describe a nanowire GAA structure that enhances device performance in terms of

- high on-state current,
- low DIBL,
- high transconductance,
- higher on/off ratio,
- steeper sub-threshold slope

2)The effect of current conduction and carrier controlling mechanisms of the device has been enhanced by using our recommended tri-layer high-k dielectric in the gate stack.

1.5 Organization of the Dissertation

As mentioned in the previous article 1.1-1.2 Barium titanate ($BaTiO_3$) is a promising ferroelectric material. So, this thesis paper involves about simulation and analysis. This simulation work is carried out in Atlas, a device simulation program created by Silvaco TCAD. This article depicts the chapter organization and the topics to be discussed.

CHAPTER II: BASICS OF GATE ALL AROUND FET

In this chapter discusses about the basic of gate all around fet. Here we discuss about the nanosheet and nanowire gate all around FET.

CHAPTER III: GAA-TFET SIMULATION TOOL & SOLUTION TECHNIQUE

This chapter discusses device simulation tools, which are software or analytical tools used to extract the IV characteristic, sub threshold slope, energy band, or other device behavior. As we used Atlas device simulation software for device simulation and performance analysis, this chapter includes basic Silvaco Atlas information. Various work windows and their analytical tools the numerical solution convergence rate and other tools associated with silvaco atlas TCAD have been briefly described.

CHAPTER IV: MATERIAL SYSTEM

This chapter discusses about the materials used in the simulation of the proposed GAA-FET. We take a look at the properties and characteristics of the materials.

CHAPTER V: DEVICE STRUCTURE AND FABRICATION

This chapter discusses about the structure and fabrication of the GAA-FET. We discuss how the GAA-FET was designed in Silvaco Atlas. We depict 2D and 3D figures of the device itself and list out parameters of each material.

CHAPTER VI: SIMULATION REASULT ANALYSIS AND DISCUSSION

This chapter examines the simulation output's characteristics and provides a theoretical explanation. This chapter also included the validation of the output electrical characteristics.

CHAPTER VII: CONCLUSION AND FUTURE WORK

This chapter contains the work's overall conclusion. The discovered improvement is highlighted.

This chapter also discusses future work.

CHAPTER 2
BASICS OF GATE ALL AROUND FET

2.1 Introduction

Gate-all-around FETs (Field-Effect Transistors) are transistors in which the gate surrounds the channel, resulting in improved electrostatic control and lower leakage current. The gate-all-around FET is made up of a nanowire channel that is surrounded by a gate. This design allows for better control of electron flow through the channel, resulting in improved performance and lower power consumption.

Furthermore, gate-all-around FETs can achieve extremely high levels of integration, making them appealing for use in future generations of electronic devices. The gate-all-around FET can be made from a variety of materials, including silicon, carbon nanotubes, and other nanomaterials. Advanced manufacturing techniques, such as precision lithography and etching processes, are required for the fabrication of gate-all-around FETs. Despite these obstacles, gate-all-around FETs are an active area of research and development and are expected to play a growing role in the future of electronics.

GAAFETs are classified into two types: vertical GAAFETs and horizontal GAAFETs. The gate of a vertical GAAFET wraps around a vertical nanowire that serves as the channel. A thin dielectric layer separates the gate from the nanowire, allowing for efficient channel control. The channel in a horizontal GAAFET is formed by a horizontal nanowire, and the gate wraps around it like a cylinder. The ability of GAAFETs to control the channel in three dimensions allows for improved electrostatics, lower leakage current, and higher device performance. The GAAFET structure also allows for better scaling because the gate can be made thinner than in traditional planar transistors, reducing short-channel effects. Moreover, GAAFETs are expected to be more resistant to process variations, potentially increasing device yield and reliability. GAAFET fabrication necessitates advanced nanofabrication techniques such as atomic layer deposition, etching, and lithography. The use of nanomaterials such as carbon nanotubes or nanowires can also present additional manufacturing challenges.

GAAFETs have the potential to become a critical building block for future generations of electronics, particularly in applications requiring low power consumption, high performance, and reliability.

However, more research is required to optimize GAAFET design and manufacturing, as well as to demonstrate their scalability and manufacturability.

2.2 I-V Characteristics Of GAAFET

The I-V (current-voltage) characteristics of a Gate-All-Around FET (GAAFET) are critical for understanding how the device behaves under various operating conditions.

The I-V characteristics of a GAAFET are determined by factors such as structure, doping profile, channel length, gate material, and others. The I-V curve of a GAAFET is similar to that of a conventional FET in general, with a linear region at low Vds and a saturation region at higher Vds. However, due to their unique geometry and properties, GAAFETs can exhibit some distinct characteristics. One of the primary advantages of GAAFETs over conventional FETs is their ability to achieve superior electrostatic control. This is reflected in GAAFETs' steeper subthreshold slope and lower drain-induced barrier lowering (DIBL). The subthreshold slope measures how steeply the current changes with respect to the gate voltage, whereas DIBL is a phenomenon in which the device's threshold voltage decreases as the drain voltage increases, resulting in less electrostatic control. By optimizing the channel geometry and doping profile, GAAFETs can achieve steeper subthreshold slopes and lower DIBL. The impact of quantum confinement effects is another feature of GAAFET I-V characteristics. As the device's channel length is reduced to the nanoscale regime, electrons become confined in the transverse direction, resulting in quantization effects that can affect device behavior. This can take the form of discrete conductance peaks in the I-V curve, known as quantized conductance, as well as other phenomena like resonant tunneling and negative differential resistance. GAAFET I-V characteristics are highly dependent on device structure and operating conditions. It is possible to achieve improved performance in terms of subthreshold slope, DIBL, and other key parameters by carefully designing and optimizing the device.

2.3 Compare and Contrast

When compared to other types of FETs, Gate-All-Around FETs (GAAFETs) have some advantages and disadvantages. Here are some examples.

2.3.1 GAAFETs vs. Planar FETs

- Advantage of GAAFETs: GAAFETs have superior electrostatic control, which results in improved performance in terms of subthreshold slope, drain-induced barrier lowering (DIBL), and gate leakage. This is due to the gate-all-around geometry's 360-degree gate control.
- Advantage of planar FETs: Simpler fabrication process, easier scaling to large sizes, and more mature technology with a longer development history.

2.3.2 GAAFETs vs. FinFETs

- Advantage of GAAFETs: GAAFETs have a more symmetric device structure with better electrostatic control, which leads to less variability in device performance. In some cases, they are also less difficult to fabricate than FinFETs.
- Advantage of FinFETs: Due to the ability to create multiple fins in the same device, FinFETs can achieve higher drive current and better short-channel behavior than GAAFETs in some cases.

2.3.3 GAAFETs vs. Nanowire FETs

- Advantage of GAAFETs: Because of the gate-all-around geometry, GAAFETs have a more uniform channel and better electrostatic control. In some cases, they may also be easier to fabricate than nanowire FETs.
- Advantage of Nanowire FETs: Because of the nanoscale dimensions of the wire, nanowire FETs can achieve better electrostatic control and lower variability than planar FETs. It is also suitable for flexible and stretchable electronics applications.

2.3.4 Why GAAFET better than the others FET

GAAFETs have some advantages over other types of FETs, making them promising for future nanoelectronics applications. Here are some of the reasons why GAAFETs outperform other FETs in certain areas:

- Superior electrostatic control: One of the main advantages of GAAFETs over other types of FETs is their ability to achieve better electrostatic control. This is because the gate-all-around geometry allows for 360-degree gate control over the channel. This results in improved subthreshold slope, drain-induced barrier lowering (DIBL), and gate leakage performance.
- Reduced variability: Because of their symmetric structure and improved electrostatic control, GAAFETs can have lower variability in device performance when compared to other types of FETs. As a result, they are appealing for high-performance and low-power applications.
- Scalability: When compared to other types of FETs, GAAFETs may be easier to fabricate and scale to smaller dimensions. This is due to the gate-all-around geometry, which provides more uniform channel doping and better gate control, allowing for better performance in smaller devices.
- Reduced power consumption: Because of their improved electrostatic control and lower variability, GAAFETs can achieve lower power consumption than other types of FETs. This is critical for applications requiring low power consumption, such as mobile devices and Internet of Things (IoT) devices.

GAAFETs have some unique advantages over other types of FETs, which make them attractive for future nanoelectronics applications. However, the choice of FET type depends on the specific application requirements and trade-offs between performance, complexity, and fabrication considerations.

2.4 Equations of GAAFET

2.4.1 The Fermi-Dirac distribution and The Newton equation

The Fermi-Dirac distribution and the Newton equation are important concepts in the physics of semiconductors and are used to describe the behavior of electrons in the channel of the Gate-All-Around FET (GAAFET).

2.4.1.1 The Fermi-Dirac distribution

The occupation of energy levels by electrons in a solid is described by the Fermi-Dirac distribution, which is a probability distribution function. The Pauli exclusion principle, which stipulates that no two electrons may occupy the same quantum state simultaneously, is taken into consideration.

The GAAFET's Fermi-Dirac distribution function can be expressed as:

$$f(E) = [1 + \exp((E - EF)/kT)]^{-1}$$

where f(E) is the probability that an energy state E is occupied by an electron, EF is the Fermi energy level, k is Boltzmann's constant, and T is the temperature.

2.4.1.2 The Newton equation

The movement of electrons in a semiconductor device is described by the Newton equation, commonly referred to as the continuity equation.

It connects the drift velocity and carrier concentration to the current density.

The GAAFET's Newton equation looks like this:

$$\partial J/\partial x = qn\mu E + qDn(\partial n/\partial x)$$

where J is the current density, q the electronic charge, n the concentration of electrons μ is the electron mobility, E is the electric field, and Dn is the electron diffusion coefficient.

2.4.2 Poisson's equation

This equation calculates the electric field and charge distribution by describing the electrostatic potential in the device's channel region.

Poisson's equation appears as follows:

$$\nabla \cdot (\varepsilon \nabla \Phi) = -\rho$$

where ε is the dielectric constant of the material, Φ is the electrostatic potential, and ρ is the charge density.

2.4.3 Current-Voltage (I-V) equation

This equation describes the relationship between the voltage applied to the gate, source, and drain terminals and the current flowing through the GAAFET.

The following equation can be used to represent the I-V equation for the GAAFET, which is comparable to that of other kinds of FETs:

$$I = \mu Cox(W/L)(VGS - Vth)^2$$

where I is the drain current, μ is the mobility of the channel carriers, Cox is the gate oxide capacitance per unit area, W and L are the width and length of the channel, VGS is the gate-source voltage, and Vth is the threshold voltage.

2.4.4 Capacitance-Voltage (C-V) equation

The capacitance of the GAAFET is described by this equation as a function of the voltage applied to the gate electrode. The fundamental electrostatics equations can be used to generate the C-V equation for the GAAFET, which is expressed as follows:

$$C = \varepsilon A/d$$

where C is the capacitance of the gate oxide, ε is the permittivity of the oxide, A is the area of the gate electrode, and d is the thickness of the gate oxide.

2.4.5 Threshold voltage equation

This equation illustrates how the gate oxide thickness, channel doping concentration, and other device characteristics affect the threshold voltage of the GAAFET. The fundamental equations of semiconductor physics can be used to construct the threshold voltage equation for the GAAFET, which can be defined as:

$$Vth = VFB + 2\varphi F + \gamma(\sqrt{2\varphi F} - qNsub/2\varepsilon si)$$

where VFB is the flatband voltage, φF is the Fermi potential, γ is a device-dependent parameter, Nsub is the doping concentration of the substrate, and εsi is the permittivity of the silicon substrate.

2.4.6 Subthreshold swing equation

The subthreshold swing, a measurement of how sharply the current fluctuates regarding the gate voltage, and the gate voltage are related to one another in this equation. Can be write the subthreshold swing equation as:

$S = (kT/q) \ln(10) (d\log(I/dVg))^{-1}$

where S is the subthreshold swing, k is the Boltzmann constant, T is the temperature, q is the elementary charge, I is the drain current, Vg is the gate voltage, and dlog(I/dVg) is the derivative of the logarithm of the current with respect to the gate voltage.

These equations are necessary for simulating the performance of GAAFETs under various operating conditions and for comprehending the behavior of electrons in the channel.

CHAPTER 3

GAA-TFET SIMULATION TOOLS & SOLUTION TECHNIQUE

3.1 Introduction

There are various device simulation tools available to simplify analysis. Here in our research work on GaAs/InN GAA-TFET with tri-layer HfO2/TiO2/HfO2 gate and BaTiO3 as ferroelectric insulator we have used Silvaco atlas Tcad for device simulation and finding some characteristics. The OriginLab has also been used for additional curve extraction, analysis, and validation.

3.2 Silvaco TCAD

3.2.1 Introduction to Silvaco ATLAS

ATLAS is a two and three dimensional Semiconductor device simulator that is physically based. It predicts or calculates the electrical behavior of specified semiconductor structures and provides information about the internal physical properties of the device. ATLAS can be used as a standalone tool for standard device simulation or as a core tool in the SILVACO VIRTUAL WAFER FAB simulation environment. Device simulation fits between process simulation and SPICE model extraction in the sequence of calculating the impact of process variables on circuit performance. ATLAS is a physics-based device simulator developed by Silvaco Inc. in the United States. It was originally designed for silicon-based MOS transistor modeling but has since been expanded with many modular extensions, making it suitable for modeling organic displays, photovoltaic cells, and many other devices. With this tool, the electrical behavior of a semiconductor device can be predicted, as can the physical process associated with device operation. The device structure will be approximated as a two or three-dimensional grid with a number of grid points, also known as nodes. A set of partial differential equations derived from Maxwell's laws and applied to these grids can be used to simulate carrier transport in the device. This method can be used to calculate performance under DC bias, AC voltage, or transient conditions.

This method can be used to calculate performance under DC bias, AC voltage, or transient conditions. Physics-based simulations are more analytical in the sense that they combine theoretical prediction with correlative knowledge. Hence it provides different result when compared to empirical which gives better approximations with the existing data and offers convenient interpolation. Physics-based simulators are less expensive and faster, and they can predict quantities that are impossible to measure. The main disadvantage is the required knowledge of device physics and the incorporation of time-consuming numerica1 procedures to solve the equations. In Atlas, the device simulation process must be specified by defining the physical structure of the device to be simulated and selecting the appropriate model equation. If the model equation is not already in the library, it can be created and included using the tool's C-interpreter function. This makes it more useful.

3.2.2 ATLAS Inputs and Outputs

Figure 3-1 depicts the different types of data that flow into and out of ATLAS. The majority of ATLAS simulations make use of two input files called command and structure file. The first input file is a text file containing ATLAS commands and syntax. The second input file is a structure file that depicts the simulated structure. ATLAS also provides three different types of output files. The first type of output file is the run time output, which displays the simulation's progress as well as error and warning messages. The log file, which saves all terminal voltages and currents from the device simulation, is the second type of output file. The solution file is the third type of output file, which saves 2D and 3D data relating to the values of solution variables within the device at a specified bias point.

DeckBuild

The DeckBuild Command window can help you to specify input files. This menu bar is found under the Commands button on DECKBUILD’s main screen. To run a simulation the type of the device structure and and its solution process should be described in DeckBuild.

TonyPlot

TonyPlot provides visualization and graphic features such as pan, zoom, views, labels, and multiple plot support of the saved data in atlas log file. TonyPlot also provides many TCAD oriented visualization functions, such as HP4154 emulation, 1D cut lines from 2D structures, animation of markers to show vector flow, integration of log or 1D data files and fully customizable TCAD specific colors and styles.

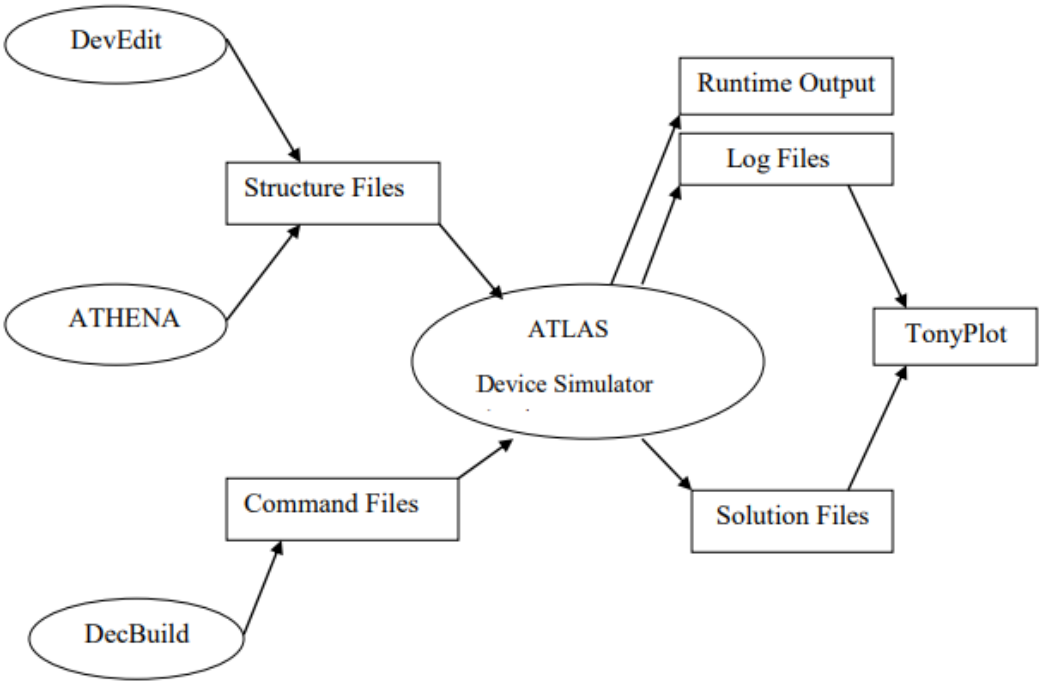


Figure 3.1 ATLAS Inputs and Outputs

3.3 Technology computer-aided design (TCAD) model

TCAD (Technology Computer-Aided Design) is a simulation software tool used to model and simulate semiconductor device physical behavior. TCAD models are based on physical principles and can accurately predict device electrical, thermal, and optical behavior. TCAD models are widely used in the semiconductor industry to design, optimize, and characterize various semiconductor devices, including GAAFETs (Gate-All-Around Field-Effect Transistor). TCAD models typically employ numerical methods to solve partial differential equations that describe the device's physical behavior.

For example, Poisson's equation is used to describe the electrostatics of the device, while the drift-diffusion equations are used to describe the carrier transport in the device. These equations are solved using numerical techniques such as finite element method, finite difference method, or Monte Carlo simulation. TCAD models can simulate various device properties, such as current-voltage characteristics, capacitance-voltage characteristics, and temperature profiles. The models can also be used to optimize device performance, such as reducing leakage current or increasing the speed of the device. Additionally, TCAD models can simulate device fabrication processes, such as ion implantation and etching, to predict the impact of process variations on device performance. TCAD models are valuable tools for semiconductor device design and optimization, as they can help reduce the design cycle time and cost. They are widely used by semiconductor companies and research organizations to simulate and optimize the performance of various semiconductor devices, including GAAFETs.

3.4 Equations used in simulation

3.4.1 Poisson's equation

Poisson's equation is used to simulate the electrostatics of the GAAFET device. It describes the relationship between the electric potential and the charge density within the device. The solution to Poisson's equation provides information on the potential profile within the device.

$$\nabla \cdot (\varepsilon \nabla \Phi) = -\rho$$

where ε is the dielectric constant of the material, Φ is the electrostatic potential, and ρ is the charge density.

3.4.2 The Newton equation

The movement of electrons in the device is described by the Newton equation, commonly referred to as the continuity equation It connects the drift velocity and carrier concentration to the current density. The GAAFET's Newton equation looks like this:

$\partial J/\partial x = qn\mu E + qDn(\partial n/\partial x)$

where J is the current density, q the electronic charge, n the concentration of electrons μ is the electron mobility, E is the electric field, and Dn is the electron diffusion coefficient.

3.4.3 The Fermi-Dirac distribution

The occupation of energy levels by electrons in a solid is described by the Fermi-Dirac distribution, which is a probability distribution function. The Pauli exclusion principle, which stipulates that no two electrons may occupy the same quantum state simultaneously, is taken into consideration.

The GAAFET's Fermi-Dirac distribution function can be expressed as:

$$T(E)\,\alpha\, exp\left(-\frac{4\sqrt{2m^{*}E_g^3}}{3\,|e|\,\hbar\,(E_g+\Delta\varphi)}\left(\frac{\varepsilon_s t_{ox} t_s}{\varepsilon_{ox}}\right)^{\frac{1}{2}}\right)\Delta\varphi$$

where, E_g, t_s and ε_s represent the energy bandgap, thickness, and dielectric constant of the semiconductor materials, respectively, and m ∗ and 1ϕ denotes the effective mass of electron and energy range, respectively, which causes tunneling.

3.5 Band-to-band tunneling (BTBT)

Band-to-band tunneling (BTBT) is a phenomenon that occurs in our GAAFET (Gate-All-Around Field-Effect Transistor) device. BTBT is a quantum mechanical process that allows electrons to tunnel through the bandgap of a semiconductor material and contribute to the device current. In this device, BTBT occurs when the gate voltage is high enough to induce a strong electric field in the channel region. In GAAFETs, BTBT can occur through two mechanisms: direct tunneling and trap-assisted tunneling. In direct tunneling, electrons tunnel directly from the valence band to the conduction band of the semiconductor material, across the bandgap. In trap-assisted tunneling, electrons tunnel through traps or defects in the bandgap, which are localized energy states within the bandgap that can facilitate electron tunneling. The GAAFET that we designed for this research uses direct tunneling.

TCAD (Technology Computer-Aided Design) simulation is used to model and simulate BTBT in our GAAFET. The simulation model is based on physical principles, such as Poisson's equation and Schrödinger's equation, and can consider the effects of BTBT on device performance. This model helps optimize device design to minimize the impact of BTBT on device performance and improve their reliability.

CHAPTER 4

MATERIAL SYSTEM

4.1 Introduction to material Used

The nanowire gate-all-around (GAA) tunnel field-effect transistor (TFET) we proposed is based on the GaAs/InN heterostructure. In the gate stacking, we used a tri-layer $HfO_2/TiO_2/HfO_2$ as a high-K dielectric and Barium titanate ($BaTiO_3$) as a ferroelectric (FE) layer. We used aluminum as contacts. The main materials of the GAAFET are Indium Nitride (InN), Gallium Arsenide (GaAS), Hafnium (IV) oxide (HfO_2), Titanium dioxide (TiO_2), and Barium titanate ($BaTiO_3$).

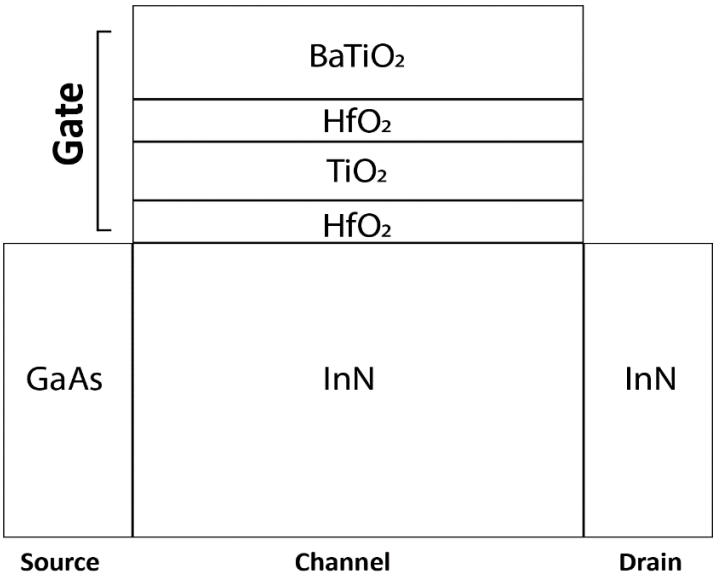


Fig. 4.1 : Schematic of the proposed GAA-FET structure

4.2 Indium Nitride (InN)

Indium Nitride (InN) is a material that has several properties that made it attractive for use in our GAAFET (Gate-All-Around Field-Effect Transistor) device.

One of the primary advantages of InN is its high electron mobility, which is the speed at which electrons can move through the material under the influence of an electric field. InN has one of the highest electron mobilities among all semiconductors, making it attractive for high-speed and high-performance applications [19].

Experimental studies have reported electron mobility values for InN in the range of 1000-4000 cm^2/Vs at room temperature, with higher values achieved at lower temperatures. However, the mobility values can vary depending on the specific measurement techniques and the quality of the material. It is worth noting that the high electron mobility in InN is attributed to its unique electronic band structure, which is characterized by a small effective mass and a high density of states at the conduction band minimum.

In addition, InN has a relatively high electron saturation velocity, which is the maximum speed at which electrons can move through the material. This makes it attractive for use in high-frequency devices like ours. Another advantage of InN is its high thermal conductivity, which is the ability of the material to conduct heat. InN has one of the highest thermal conductivities among all semiconductors, making it ideal for use in high-power our application where heat dissipation is a concern. InN also has a narrow bandgap, which is the energy difference between the valence band and the conduction band of the material. Several theoretical calculations have suggested that the intrinsic bandgap of InN is around 0.7-0.8 eV, which is in the range of the optimal bandgap for GAAFET applications [20].

Overall, the combination of high electron mobility, high thermal conductivity, and narrow bandgap makes InN an attractive material for use in our nanowire GAAFET device.

4.3 Gallium Arsenide (GaAS)

One of the primary benefits of GaAs is its high electron mobility, which is the rate at which electrons can move through the material when subjected to an electric field. Because GaAs has higher electron mobility (5000-8500 cm^2/Vs at room temperature) than silicon, it is appealing for high-speed and high-frequency applications. Furthermore, GaAs has a relatively high electron saturation velocity, which is the fastest electrons can travel through the material. As a result, it is appealing for use in high-frequency devices. Another advantage of GaAs is its large bandgap (1.42 eV at room temperature),

which is the energy difference between the material's valence and conduction bands. Because of its wide bandgap, it has high breakdown voltages and low leakage currents, making it appealing for use in power electronics[21]. GaAs has a high electron velocity, or the average speed at which electrons move through the material. As a result, it is appealing for use in high-performance devices such as our GAAFET. GaAs-based GAAFETs have demonstrated promise in high-frequency and high-power applications such as RF and power electronics. GaAs-based GAAFETs, on the other hand, can be more expensive to manufacture than silicon-based devices, and GaAs is not as widely used in the semiconductor industry as silicon. As a result, the use of GaAs in GAAFETs may be restricted to specialized applications where the performance benefits justify the higher cost.

Overall, GaAs is an appealing material for use our GAAFET devices due to its high electron mobility, wide bandgap, and high electron velocity.

4.4 Hafnium Oxide (HfO_2)

HfO2 (hafnium dioxide) is a popular material used in the gate dielectric layer of GAAFETs (Gate-All-Around Field Effect Transistors) for several reasons. HfO2 has a high dielectric constant (k~25), which allows for a greater gate capacitance per unit area. This is important because a higher gate capacitance leads to improved control over the channel charge density, enabling better transistor performance. HfO2 also has good interface properties with InN, which means it can form a stable and low-defect interface with the InN channel of the GAAFET. This is important because a high-quality gate dielectric interface is necessary to minimize leakage current and improve device reliability [22]. HfO2 is thermally stable up to high temperatures, which is important for device fabrication processes that require high-temperature processing steps.

Because of its high dielectric constant, good interface properties, thermal stability, and radiation hardness, HfO2 is chosen for the gate dielectric layer in our GAAFET. These properties all contribute to improved device performance and reliability.

4.5 Titanium dioxide (TiO_2)

TiO2 (Titanium dioxide) is also a popular material used in the gate dielectric layer of GAAFETs (Gate-All-Around Field Effect Transistors), and it has some unique properties. TiO2 has a wide bandgap (3.2 eV) and high resistivity, which leads to low leakage current in the gate dielectric layer. This is important for reducing power consumption and improving device performance. TiO2 has a high dielectric constant (k~80), which allows for a greater gate capacitance per unit area, similar to HfO2. It is chemically stable and does not react with other materials commonly used in semiconductor fabrication. The properties of TiO2 can be tuned by adjusting its stoichiometry or by doping with other elements, which provides flexibility in optimizing its electrical properties for different device applications.

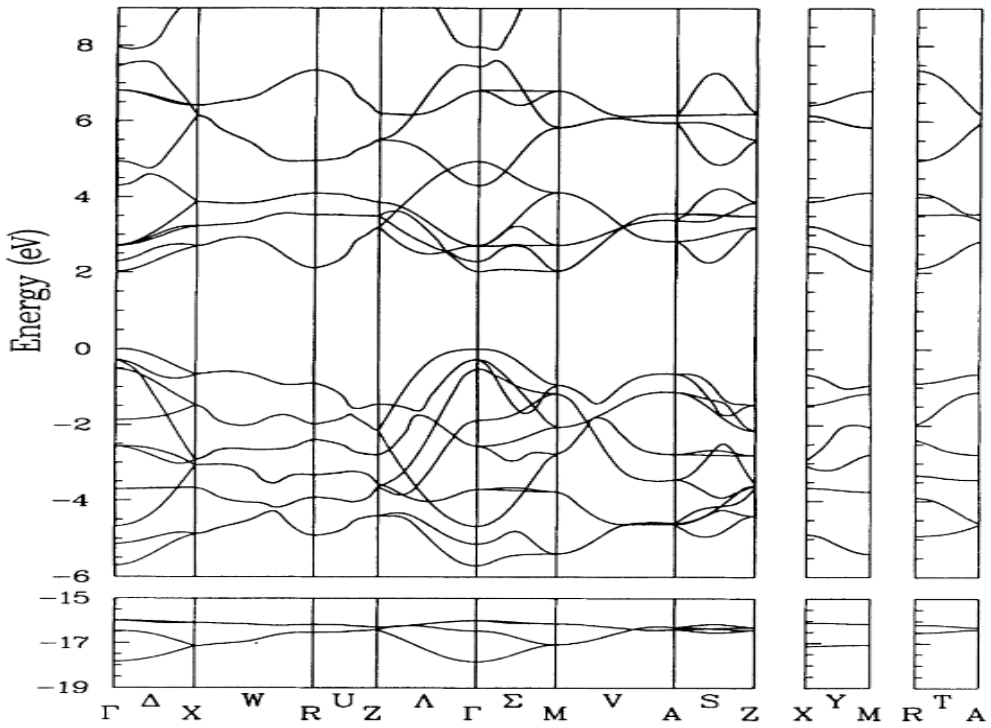


Fig.4.2: Ti02 band structure along the irreducible Brillouin zone's high-symmetry directions. The valence-band maximum is assumed to be the energy zero[23].

4.6 Barium titanate ($BaTiO_3$)

BaTiO3 (barium titanate) is a type of material that exhibits ferroelectric properties, which means it can have a permanent electric polarization that can be switched by an external electric field. This property makes it a suitable material for use in gate-all-around field-effect transistors (GAAFETs). In GAAFETs, BaTiO3 is used as a gate oxide material. The gate oxide is a thin layer of material that separates the gate electrode from the channel region of the transistor. When an electric field is applied to the gate oxide, it controls the flow of current through the channel region, allowing the GAAFET to function as a switch. BaTiO3 is particularly useful for this application because its ferroelectric properties allow it to maintain a stable electric polarization even in the absence of an external electric field. This means that the gate oxide can be operated at low voltages and still provide a strong electric field to control the channel region of the transistor. Additionally, BaTiO3 has a high dielectric constant, which allows for better gate control and faster switching speeds [24].

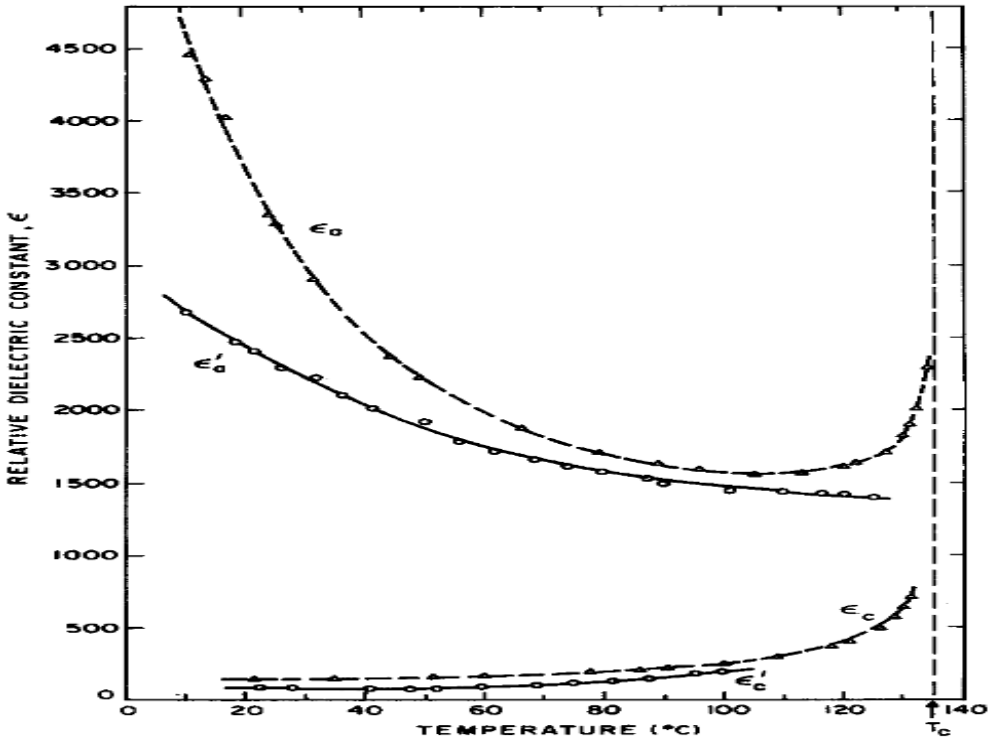


Fig.4.3: The dielectric constant of melt-grown single-domain BaTiO3 is temperature dependent. In the tetragonal phase, along the a and c axes. E and l represent unclamped a and c axis values at 100 kHz, while cf and r represent clamped a and c axis values at 250 MHz

BaTiO3, or barium titanate, has been shown to exhibit negative capacitance behavior under certain conditions. This behavior is related to the intrinsic properties of the material, such as its polarization and dielectric constant. When BaTiO3 is subjected to an external electric field, the polarization of the material changes in response to the field. At a certain critical field strength, the polarization can become unstable and undergo a phase transition to a new state with a lower energy. In this new state, the dielectric constant of the material is negative, leading to the negative capacitance behavior. The negative capacitance effect in BaTiO3 has potential applications in electronics, particularly in improving the performance and energy efficiency of our GAAFET device[25].

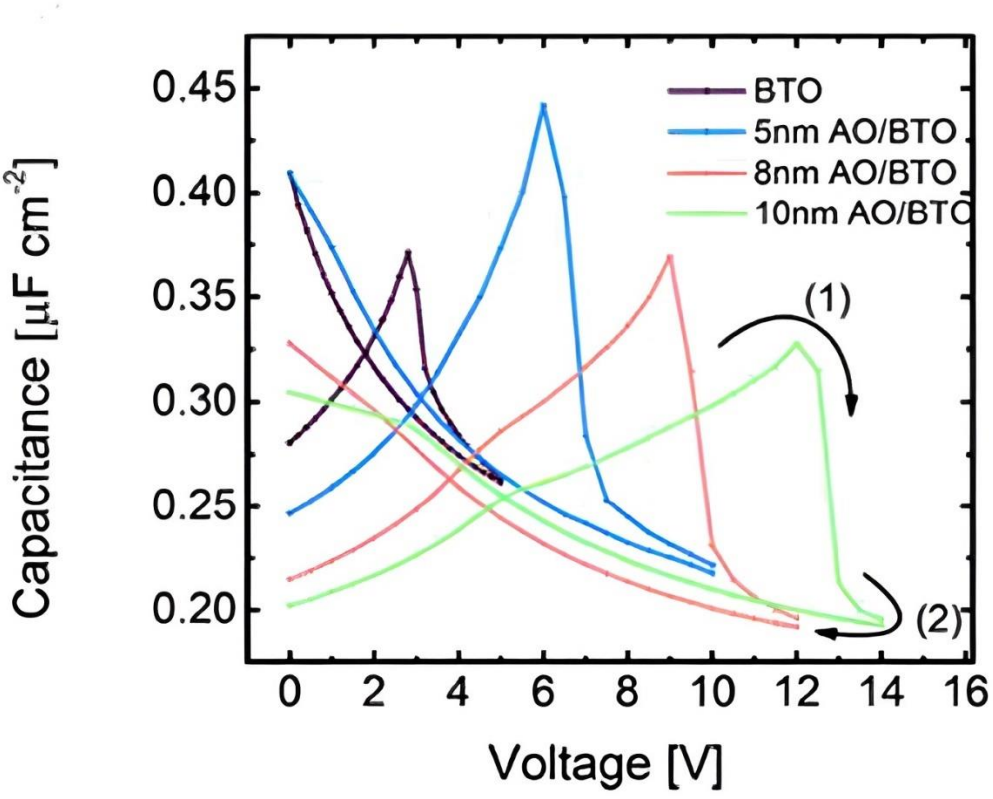


Fig.4.4: Negative capacitance of $BaTiO_3$

CHAPTER 5

DEVICE STRUCTURE AND FABRICATION

5.1 Present trends in GAAFET Structure

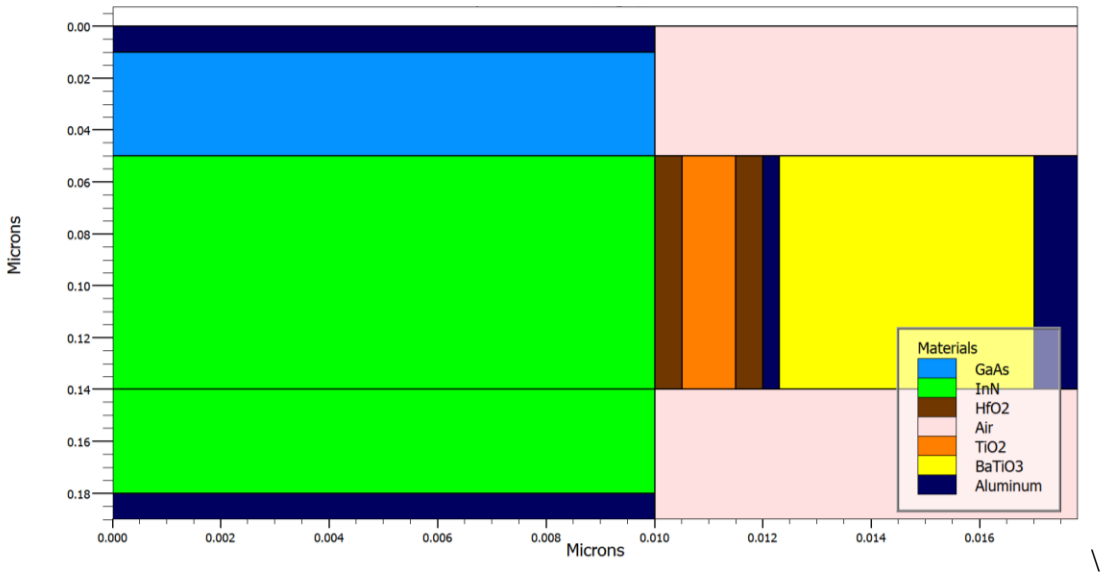
As stated previously, GAAFET (gate-all-around field-effect transistor) has gained a lot of attention in recent years due to its potential to overcome the limitations of conventional planar transistors. As technology advances, there are several trends in GAAFET structure that are emerging. One trend in GAAFET structure is the use of nanowires as the channel region. This allows for better electrostatic control of the channel and improved gate control. Nanowires can also be easily integrated into a 3D structure, which is ideal for GAAFETs. Another trend is the use of stacked nanosheets as the channel region. This structure provides a larger surface area for the channel, which results in improved performance. It also allows for better scalability and easier integration into existing fabrication processes. Heterojunction GAAFETs incorporate different materials with different electronic properties into the device structure. This allows for improved device performance, such as faster switching speed and lower power consumption. Vertical GAAFETs are structures where the channel region is oriented vertically rather than horizontally. This structure allows for better electrostatic control of the channel and improved gate control.

5.2 Device Architecture

Fig. 5.1 shows the suggested device architecture (2D & 3D) as well as the equivalent capacitance model. The entire GAA TFET structure is shown here. We used 10 nm as the GaAs/InN nanowire radius in the TFET construction (R). The gate's (LG), drain's (LD), and source's (LS) respective lengths are 90 nm, 50 nm, and 50 nm. The additional structural variables used in this architecture are displayed in Table 1 and are highly precise and logical. For triggering high dielectric gate oxide on the InN channel,

we proposed a novel tri-coating structure with TiO2 (εTiO2 ≈ 80) interleaved between two layers of HfO2 (εHfO2 ≈ 25). Finally, a layer of BaTiO3 is added to the tri-layer gate with a thickness of 5nm. Aluminum is used as contact for the device.

(a)



(b)

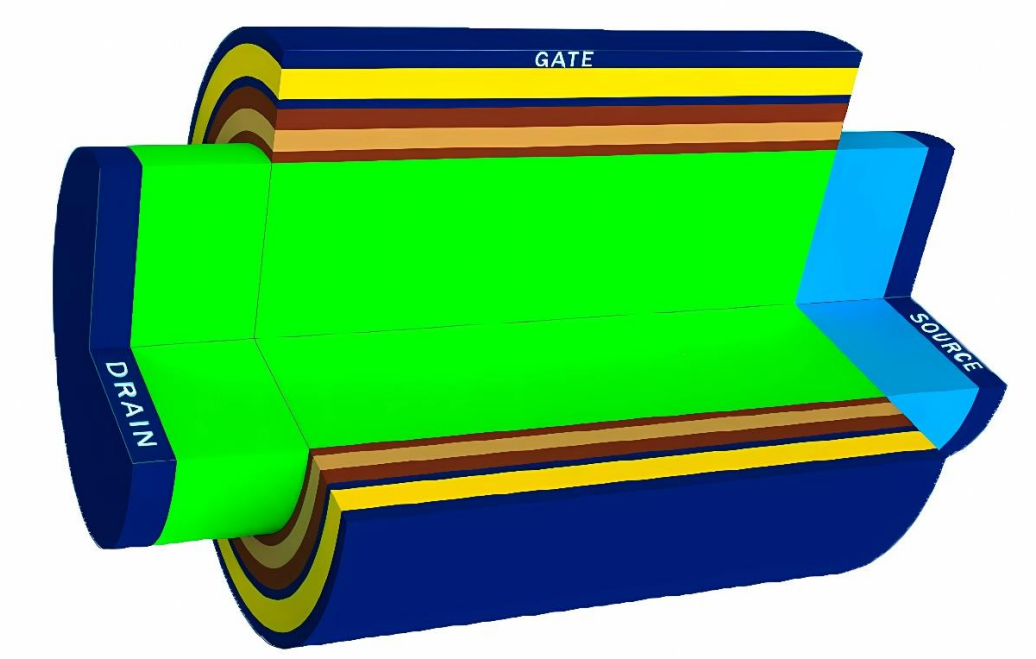


Fig 5.1: (a) Silvaco 2D outlook of GaAs/InN nanowire gate-all-around with tri-layer gate and $BaTiO_3$ ferroelectric. (b) 3D view of the NW CGAA-FET.

Table 5.1: Parameters of the proposed NW GAA-TFET

Parameter Name	***Value***
Nanowire radius	10 nm
Length of gate	90 nm
Length of drain	50 nm
Length of source	50 nm
High-K gate oxide thickness ($HfO_2/TiO_2/HfO_2$)	0.5 nm + 1 nm + 0.5 nm
Dielectric constant of HfO_2	25
Dielectric constant of TiO_2	80
Source and drain contact (Al)	5 nm
Gate contact (Al)	1.5 nm
Ferroelectric ($BaTiO_3$) thickness	5 nm
Source doping concentration	1 x 10^{19} /cm^3 (p - type)
Drain doping concentration	1 x 10^{19}/cm^3 (n - type)
Channel doping concentration	1 x 1015/cm^3 (n - type)
Gate work function	4.06 eV

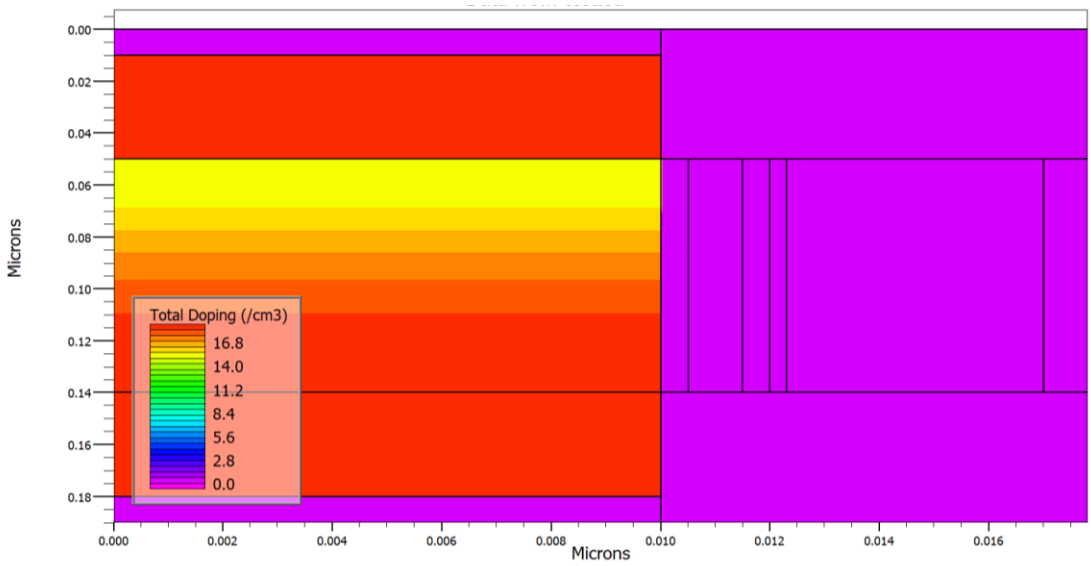


Fig 5.2: Doping profile of the proposed GAAFET

CHAPTER 6

SIMULATION REASULT ANALYSIS AND DISCUSSION

6.1 Result extraction

We have familiarized ourselves with the proposed structure of the cylindrical GAA-FET's design, architecture, and simulation technique in the previous chapters. Now, after running the simulation a number of times in Silvaco Atlas with differing values will get output curves and bias info in TonyPlot. From TonyPlot we can save the results as a csv (comma separated value) files, which we can plot using a plotting software. We used OriginLab (Origin Pro) to plot out the output files and get the curves we require for the evaluation of our GAA-FET device.

6.2 Band to Band Tunneling phenomenon

Fig. 6.1 and Fig 6.2 shows the relevant energy band diagrams of the GaAs/InN heterojunction with a broken gap alignment that forms in the source to channel region. As seen, in order to cause the tunneling phenomenon, the gate voltage must be increased. This narrows the conduction band and causes a corresponding tunneling current to emerge. This enables carriers to tunnel from the valence band into the conduction band at the source end of the channel side and then to the device's drain section.

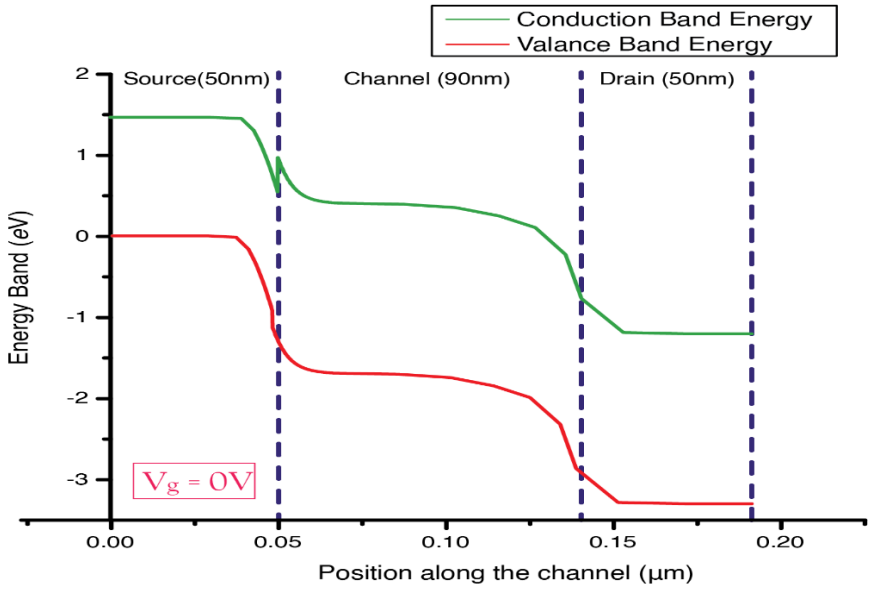


Fig. 6.1: Energy band diagram of the proposed GAA-FET in OFF-state

Due to the high barrier width in the source-to-channel junction under the OFF-state condition (V_g = 0 V and V_d = 0.5 V), as shown in Fig. 6.1, there is no tunneling current, which means more energy is required to tunnel electrons from the valence band of the source into the conduction band of the channel region.

When a voltage is given to the gate that is greater than the threshold voltage, the applied electric field pulls on the conduction band, causing the conduction band to bend downward.

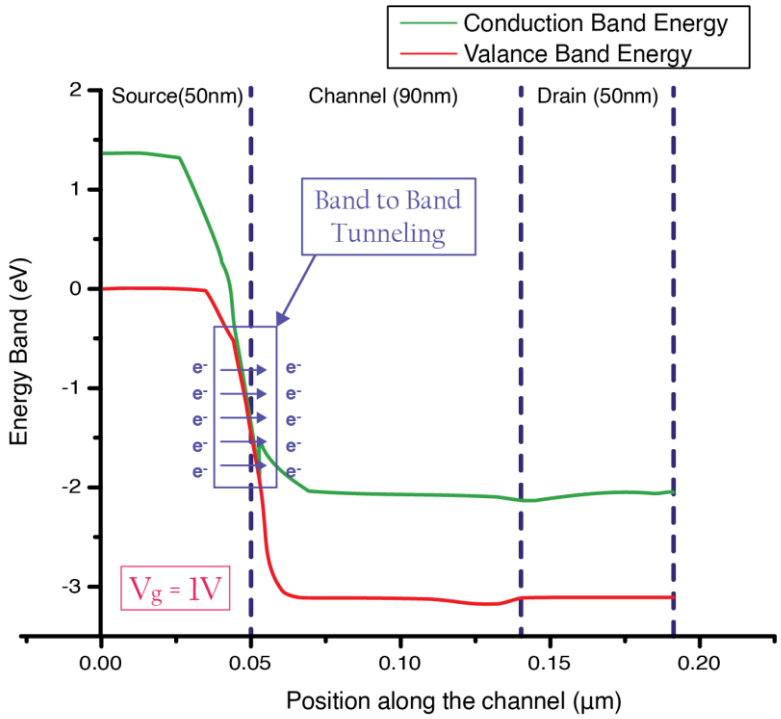


Fig. 6.2: Energy band diagram of the proposed GAA-FET in ON-state

The appropriate energy band bending structure of the nanowire GAA TFET is illustrated in Fig. 6.2 under the ON-state condition (Vg = 1 V and Vd = 0.5 V).

It shows that the conduction band bends downward due to the strain caused by the supplied gate voltage, lowering the energy spectrum. The charge density in the source-to-channel junction increases as well, resulting in a narrowing of the barrier. The alignment was chosen to provide the following energy band diagram, which allows for a high drain current value.

Because of this alignment, the prohibited energy gap will be large enough to generate a low current value in the devices off state while remaining compact enough to provide a significant amount of current in the device's on state, which will be a significant benefit.

6.3 Current density and e-tunneling

Figures 6.3 and 6.4 show the distribution of current density and e-tunneling rate in the band bending region for both the off-state and on-state conditions of this device. The barrier width decreases in the on-state due to improved coupling between the gate and the channel. Furthermore, as charge density increases from the source region to the channel region, the electric field increases.

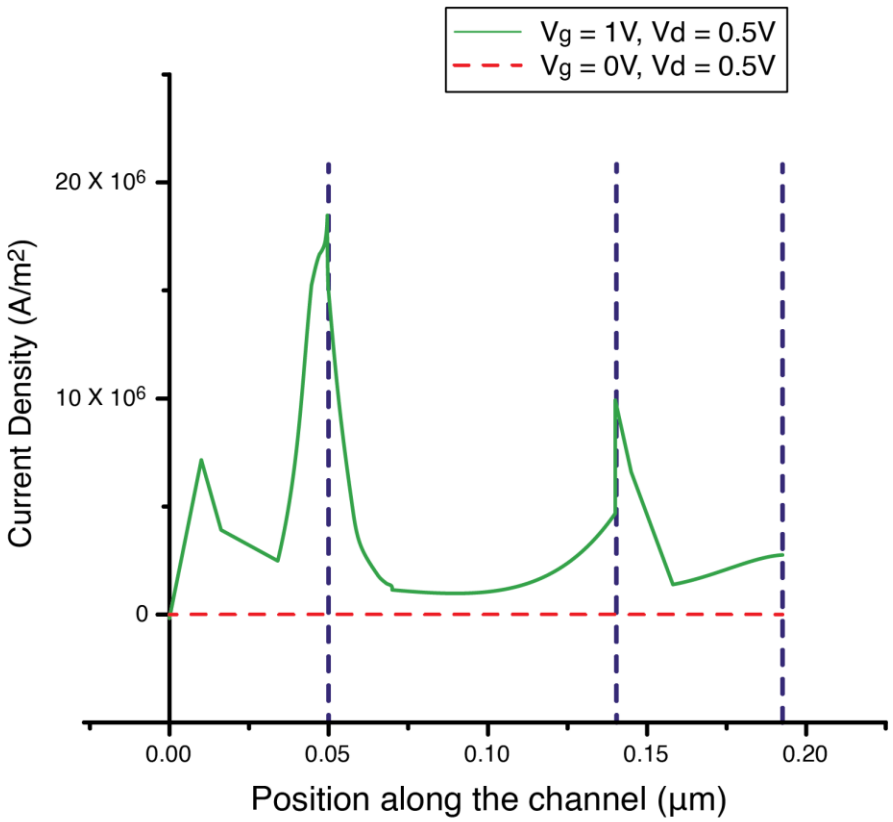


Fig 6.3: Current density curve of the GAA-FET device

When the device is turned on, the current density is formed laterally near these two junctions, as shown in Fig. 6.3. As a result, electron localization at the source end increases, and peak tunneling of those electric fields occurs.

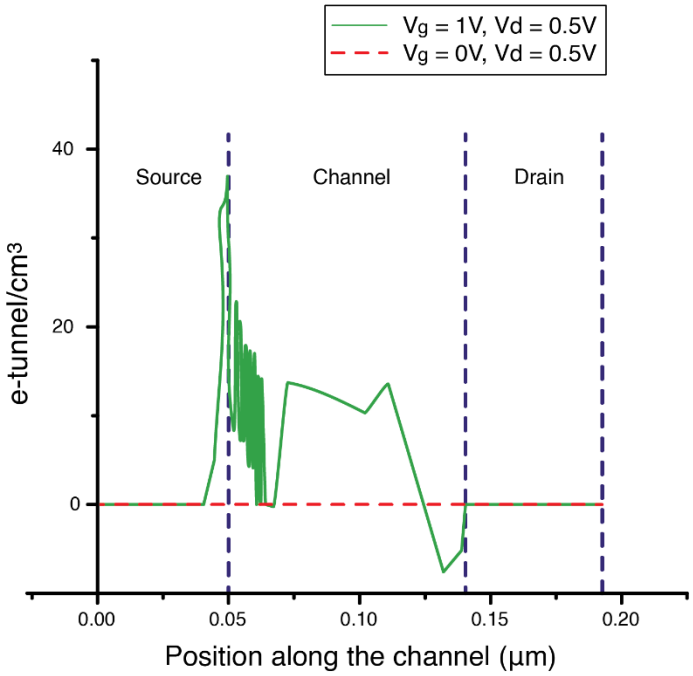


Fig. 6.4: e-tunneling graph of the GAA-FET device

Hence, the BTBT rate in the source-to-channel junction increases, as shown in Fig. 6.4. Because the transmission through the barrier can be finite and vary exponentially, the wavefunction in the on-state may vanish on the channel to the drain side and return on the source to the channel side.

The red dashed line in Figs. 6.3 and 6.4 indicates that the device is in an off-state state, and thus no tunneling occurs.

6.4 Transfer characteristics

The transfer characteristics of a transistor is a graphical representation of the relationship between the input voltage and the output current (Ic or Id) of the transistor. It describes how the input signal applied to the base or gate of the transistor affects the output current flowing through the collector or drain of the transistor.

In the case of our field-effect transistor, the transfer characteristics can be described by the input characteristic curve, which shows the relationship between the drain-source current (Ids) and the gate voltage (Vg) for different values of the drain voltage (Vd).

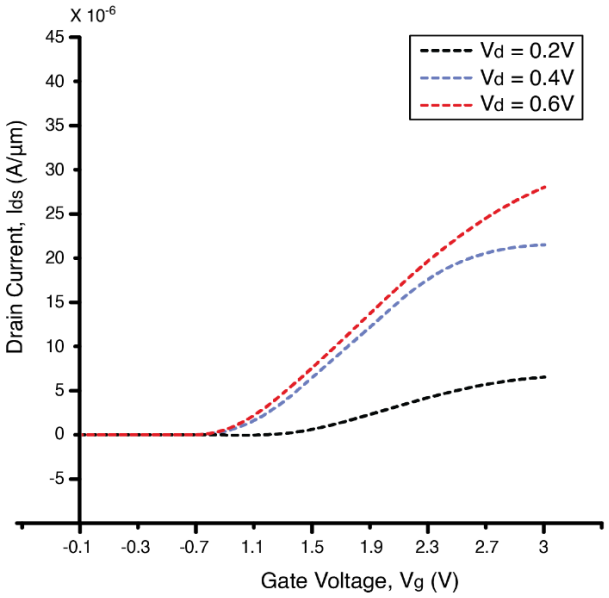


Fig. 6.5 : I_{ds} vs. V_g Transfer characteristics of the proposed GAA-FET

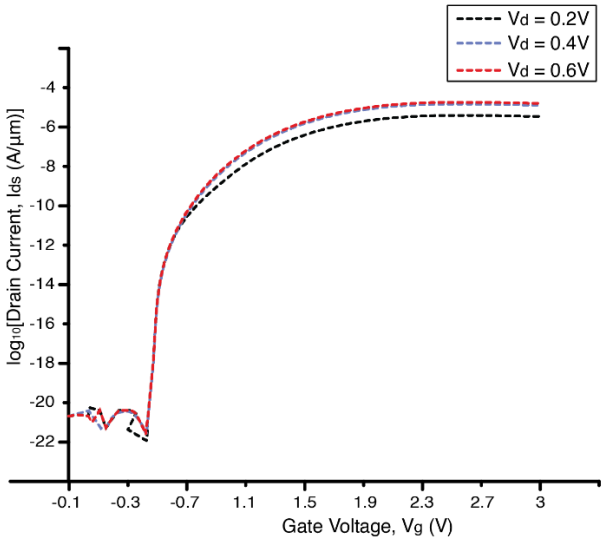


Fig. 6.6 : $\log_{10}(I_{ds})$ vs. V_g Transfer characteristics of the proposed GAA-FET

A 0.2 V step voltage is used to change the drain voltage (Vd) from 0.2 V to 0.6 V. As previously stated, traditional TFET structures have a low on-state current. The proposed baseline heterostructure, on the other hand, has an on-state current of 27 μA and a high ON-OFF ratio of 1.831 x 10^9. Furthermore, increased drain voltage results in a high on-state current, indicating good carrier conduction control. The threshold voltage is V_g = 0.95 V at V_d = 0.6 V. Also, the proposed NGAA-TFET has a lower DIBL value ($\frac{V_{th}^{0.4V} - V_{th}^{0.6V}}{0.6-0.4}$) of 13 mV because the drain field effect may be minimized by the screening action of the resultant depletion area. In conjunction with the InN channel, the GAA design provides improved control over carrier conduction.

6.5 Subthreshold swing

Subthreshold swing (SS) is a key parameter that characterizes the performance of a transistor in its subthreshold region, where the drain current is very small. It measures how much the gate voltage needs to be changed to produce a ten-fold change in the drain current. A lower subthreshold swing indicates better performance, as it means that the transistor can switch on and off more efficiently with lower power consumption. Gate-All-Around FETs (GAAFETs) have demonstrated excellent subthreshold swing due to their unique structure and operation. The gate surrounds the entire channel, which allows for better electrostatic control of the channel and reduces the effects of short-channel effects, such as drain-induced barrier lowering (DIBL) and hot carrier injection.

The subthreshold swing of a GAAFET can be calculated using the following equation:

$SS = (kT/q) \times \ln(10) \times (C_{ox}/C_{eff})$

Here, k is the Boltzmann constant, T is the temperature, q is the electronic charge, C_{ox} represents the gate oxide capacitance per unit area, and C_{eff} is the effective channel capacitance.

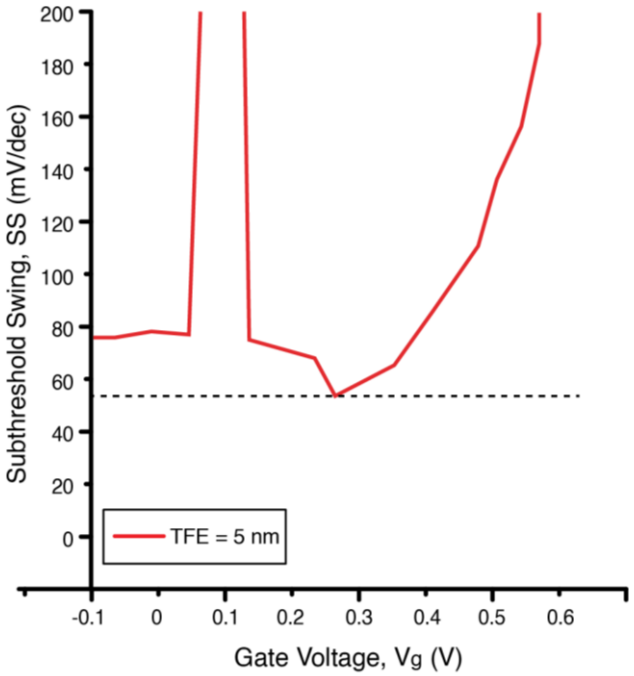


Fig. 6.7: Subthreshold swing graph of the device

The Subthreshold swing for the proposed nanowire gate-all-around GaAs/InN tunnel-FET at 5 nm $BaTiO_3$ thickness is shown in Fig. 6.7.

The steepest slope in the graph can be seen at 55 mV/dec.

6.6 Transconductance

Transconductance is a measure of how much the drain current of a transistor changes with respect to the gate voltage. It is an important parameter that characterizes the performance of a transistor.

For Gate-All-Around FETs (GAAFETs), the transconductance can be expressed as:

$$gm = (2muC_{ox} \times (V_{ds}-V_{th}))/L$$

Where, mu is the electron mobility in the channel, C_{ox} is the gate oxide capacitance per unit area, V_{ds} is the drain-source voltage, V_{th} is the threshold voltage, L is the channel length.

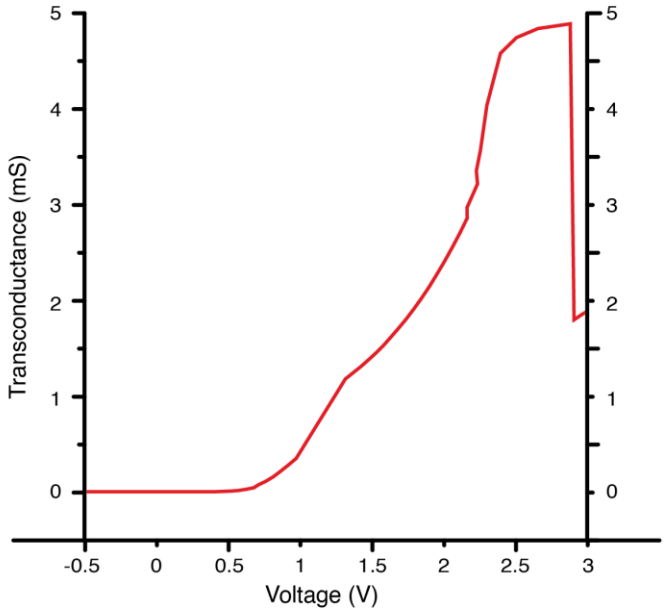


Fig. 6.8: Transconductance (mS) vs Gate voltage graph of the proposed GAA-FET

The transconductance of the proposed gate-all-around TFET with a 5nm thick layer of BaTiO3 is shown in Fig. 6.8. The TFET with the tri-layer dielectric (HfO2/TiO2/HfO2) has the highest transconductance value at 4.92 mS, indicating a significant improvement in transconductance characteristics when compared to prior works.

6.7 Discussion of Simulated output

With the simulation and extraction of various performance parameters of the proposed GAA-TFET complete. The current study's findings are compared to those of previous studies, as shown in Table 6.1.

Table 6.1: Comparison of previous investigations with that of the current study.

Performance Parameters	**Current work**	**Prior works**
On State current	27.5 μA	1.867 mA[26], 15 μA[12], 10 mA[13]
On to Off ratio (I_{ON}/I_{OFF})	1.831×10^9	10^7[12], 10^{10}[26], 10^6[13]
Sub-Threshold Swing	55 mV/dec	55mV/dec for Arsenene & Antimonene[26],39mV/dec for WTe_2[26], 15mV/dec[14],30mV/dec[27],>60 mV/dec[13]
DIBL	13 mV	65 mV[28]
Transconductance	4.92 mS	≈ 3 mS[13]

As seen from the table, the proposed GAA-TFET with a high dielectric tri-layer of HfO2/TiO2/HfO2 and a 5 nm BaTiO3 layer significantly improves overall device performance specially in lowering the DIBL and increasing the transconductance.

CHAPTER 7
CONCLUSION & FUTURE WORK

7.1 Conclusion

In conclusion, the GaAs/InN baseline TFET and a ferroelectric layer ($BaTiO_3$) in the gate stack are combined to show a hybrid nanowire GAA TFET structure. The fractured and staggered bandgap alignment is made possible by the employment of massive lattice-mismatched materials, and the GAA structure preserves the device's superior current conduction and carrier management capabilities. The maximum I_{ON} /I_{OFF} ratio of TFET is achieved by adjusting the ferroelectric gate insulator and GAA TFET channel architecture to provide the best band-to-band tunneling and potential amplification. A higher on-state current of roughly 27.5uA and an I_{ON}/I_{OFF} ratio of the order of 1.831×10^9 produced by the revised device structure demonstrate the CMOS devices' improved channel control and current control capabilities. The lowest SS of 55 mV/dec is attained with a 5 nm $BaTiO_3$ in the gate stack, making this TFET structure promising as energy-efficient switches. A significant transconductance (gm) of 4.92 mS, a DIBL of 13 mV, and a threshold voltage of 0.95V are also revealed in the output characteristics. which stand out when compared to all other cutting-edge TFETs. The proposed GaAs/InN nanowire gate completely encircles the TFET, alleviating scaling-down restrictions and lowering power consumption.

Consequently, GaAs/InN nanowire GAA TFET appears to be a promising solution for an Internet of Things (IoT) technological platform, providing a distinctive path for the continued expansion of the application of electronic gadgets.

7.2 Future Work

The following features can be investigated to learn more about the real-time performance of this nanowire cylindrical GAA-TFET:

1. Investigation of different source materials with lower bandgap.

2. Improvement in simulation technique.

3. Integration with existing technologies.

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