REAL TIME IMPLEMENTATION OF CDMA ENCODING-DECODING BY TMS320C50 DSP KIT

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Abstract: *The steadily decreasing cost of wireless communications and its growing development have resulted in its increased popularity. But the drawback here is to limited bandwidth of transmission medium and multipath interference. So an important challenge in wireless system design is the selection of an appropriate multiple-access scheme. Among many multiple access strategies developed so fa ,**CDMA** (Code Division Multiple Access) based on IS 95 plays an important role. CDMA encoding and decoding is the main feature of CDMA system and it also takes a significant amount of time because of spreading the original signal. So an efficient hardware is necessary for encoding and decoding .This paper includes the **CDMA** encoding and decoding technique and its real time implementation by **TMS320C50 DSP KI** .*

Keyword: *Walsh, TMS320C50, AIC, Implementation, DSP.*

1. Introduction

In CDMA all the subscribers use the same large frequency band and it is the main power of CDMA. With Code Division Multiple Access, network stations transmit continuously and together on the same frequency. For each user in CDMA , there is an unique signature code that consists of a binary sequence. Interference between the transmissions of different users is resolved by the signature code.

It is analogous to a hall room where all couples can speak together by using different languages. Each person only receive desired language from others and reject other's language as noise .

At first generation an analog system Advanced Mobile Phone System (AMPS) used FDMA [3].Here voice can be transmitted through dividing the total frequency into several cells. When digital system came then it used both TDMA [3] and FDMA. Here frequency band is further divided into time slots. As transmission frequency band is limited so a fixed amount of user can communicate at a time. For additional users call fail occurs [7]. As CDMA can reuse frequency by coding theory it can handle additional user load. In CDMA system original signal is spreaded into a wide band [5] signal that is called encoding and reverse is called decoding .Here all the input signals represented into a fixed wide band signal .Although signals are transformed into a fixed large frequency signal , yet signal can't interfere one another because of CDMA encoding system. CDMA encoding system use a orthogonal [3] code named walsh [1] code for encoding and decoding.

CDMA can offer 7 to 10 times the capacity of analog technologies and up to 6 times the capacity of digital technologies such as TDMA. As all the users can use total frequency at a time , data speed of CDMA system is several times higher than previous one. CDMA provides 144 Kbps speed for mobile users and 2 Mbps [1] for stationary users. So to handle this high speed data transmission and reception choice of hardware is an important factor. In this work TMS320C50 DSP kit [6] has been used for encoding and decoding. This hardware device is capable of real time CDMA encoding and decoding because of its high clock speed. At the first look signal spreading and depreading is shown and then implementation details of TMS320C50 kit is represented in the later part of this paper.

2. Direct Sequence Spread Spectrum

Direct Sequence spread spectrum achieves band spreading by spreading the information

symbol stream with a higher rate chip sequence [4]. Each symbol of duration T_s is spread into multiple chips of chip duration $T_c<T_s$. The bandwidth expansion factor , $L = T_S / T_C$ determines the amount of redundancy infected during spreading. L is often called the "spread factor". Spreading the spectrum take place by multiplying each symbol information by its chip sequence. Mathematically, the spread spectrum modulated signal can be expressed as follows [5]:

$$X(t) = \sum_{k=-\infty}^{\infty} S(k) W_k (t - kT) \qquad (1)$$

Where, $S(k)$ = kth symbol of information stream

$W_k(t)$ ="spreading waveform" or "signature waveform" for k[th] symbol.

This chip sequence is further expressed as follows [5]:

$$W_k(t) = \sum_{i=1}^{L} C_k(i) P(t - iT_C + T_C) \quad (2)$$

Where , $C_k(i)$ = each chip of spreading waveform. $P(t)$ = chip pulse shaping filter .

Original signal can be recovered by multiplying the spreading sequence by signature waveform.

2.1 Walsh Code

In DS-CDMA system walsh code is used as the signature waveform. The walsh code is calculated from a special type of matrix called walsh matrix. Each row of this matrix corresponds to a walsh code and each code is unique. Each code is a sequence of 1 and -1 . These 1 and -1 are called chips of walsh code. A walsh matrix contains one row of all ones and the remaining rows each have equal number of ones and minus ones. Walsh code also called Hadamard code [1]. IS-95 CDMA [2] system uses a 64 X 64 walsh matrix for walsh code generation. Each row of the matrix indicates a specific walsh code. Each walsh code consists of 64 chips. Each CDMA user is assigned a walsh code for spreading his bit stream. So only 64 user is possible in this system. Walsh code can be generated using following function:

$$W_{2n} = \begin{bmatrix} W_n & W_n \\ W_n & \overline{W}_n \end{bmatrix} \quad \text{where,} \quad W_1 = [1]$$

So, $W_2 = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$ (3)

Where n is a power of two and W_n is the information of $\overline{W_n}$ such that 1 becomes -1 and -1 becomes 1.

2.1.1 Properties of Walsh Code

Orthogonality of each pair of walsh code is an important property that make it popular for CDMA encoding and decoding . This property indicates that bit wise multiplication and summation of each pair of walsh code is zero. This is expressed mathematically as follows [2]:

$$\sum_{i=1}^{i=m} W_{a,i} * W_{b,i} = 0 \quad (4)$$

Where, $W_{a,i}$ = ith chip of a's Walse code and $W_{b,i}$ = ith chip of b's Walse code.

Example: (1 -1 1 -1) * (1 1 -1 -1)
= (1 – 1 – 1 + 1) = 0

If two same walsh code is bit wise multiplied and summed then result is number of chip in that code. Again if a code is bitwise multiplied and summed with negation of code then result is same as previous but negative signed. These are expressed mathematically as follows [3]:

$$\sum_{i=1}^{i=m} W_{a,i} * W_{a,i} = m \quad \text{and}$$

$$\sum_{i=1}^{i=m} W_{a,i} * \overline{W}_{a,i} = -m \qquad (5)$$

Using walsh code spreading and despreading is performed as follows-

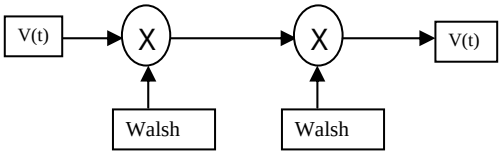

Fig.1. Spreading and dispreading

3. Implementation

Implementation means physical representation of any logical system. So implementation is related with real world. Here real world data is encoded and decoded by a hardware. All the processing is performed in the processor of the hardware but before processing analog interface

between the hardware and real world need to establish. So implementation includes two parts:

1. Analog interfacing
2. Encoding and Decoding.

3.1 Analog Interfacing

In implementation TMS320C50 DSP kit is used as hardware device which clock speed is 40 MHz [6]. At the first step of implementation signal need to input in the kit. There are two ways of getting input and sending output in this DSP kit:

1. Interfacing by the A/D and D/A converter.
2. Interfacing by AIC chip.

3.1.1 Interfacing by A/D and D/A Converter

DSP kit has onboard analog to digital converter (A/D) ADS7805S [6] and a digital to analog converter (D/A) DAC712 [6]. Both the converters are 16 bit. Sampling frequency can be set by adjusting delay between two successive data acquisition and data transmission.

Both A/D and D/A converters have five pins where one is used for grounding purpose and another four pin can be used for interfacing four signals.

Fig.2 Pin configuration of A/D and D/A.

In this word only one pin of A/D converter is used to get input an analog voice signal and one pin of D/A converter is used for sending analog output to the realworld.

3.1.1.1 Adjusting Sampling Frequency

If a signal need to sample at 1 KHz ,then A/D or D/A have to wait 1000 cycle to take the next sample. Generally input and output operation is performed inside a user defined function. Then for 1KHz sampling function need to take exactly 1000 cycle to execute. If less than 1000 cycle is needed for instructions inside function then delay is imposed in the function to adjust sampling frequency so that-

Instruction cycles + delay cycles =1000 cycles

Here it need to mention that clock rate of DSP processor is 40 MHz.

For our work only a pin is used. Conversion take place by executing following code-

A/D conversion	D/A conversion
Data_Digital = ADC	DAC1 = Data_Digital DAC2 = Data_Digital

Where ADC is the port address of A/D and DAC1 and DAC2 are port address of D/A converter.

When " Data_Digital = ADC " [6] instruction is executed , a 16 bit sample data from A/D converter pin is stored in the user defined variable named Data_Digital. Again when "DAC1 = Data_Digital" and "DAC2 = Data_Digital" [6] instructions are executed then 16 bit data from variable Data_Digital is converted to it's analog equivalent and transferred to the real world through D/A pin.

3.1.2 Analog Interface By AIC

TMS320C50 DSP kit [6] has on board Analog interface chip (AIC). It's number is TLC32040 [6]. It is used to get analog input input from real world. This chip is specially used for audio processing .TLC32040 is a 20 pin chip. The main pins are DR, DX, IN+, AUX IN+, OUT+ e.t.c. DR and DX pins are used for serial port data receive and transmit respectively. The main features of AIC are as follows-

1. AIC have two input channels - IN+ and AUX IN+.
2. IN+ pin is internally connected to a RCA connector called audio in which is used to get input from microphone.
3. OUT+ pin is internally connected to the RCA connector [6] called audio out port which is used to interface with speaker.
4. AIC has a 14 bit A/D and 14 bit D/A converter.
5. Sampling rate of AIC can vary upto 19.2 KHz depending on the value of master clock and the resister value TA and TB. Default sampling frequency is 16 KHz
6. Serial data transfer occurs by XINT and RINT interrupts. Signal is received and transmitted by executing function rint() and xint() respectively. Inside rint() function Data Receive Resister (DRR) is assigned to a digital variable and inside xint() Digital data is assigned to the Data Transmit Register (DXR). Here it need to be note that these two functions execute when RINT and XINT interrupt is thrown.
7. AIC has a band pass input filter and a low pass switched capacitor output filter.

8. AIC has analog internal voltage reference.
9.Input range of AIC is generally -6v to 6v but it can be changed.
The following figure shows the flowchart [9] of Analog interface with TLC32040 AIC:

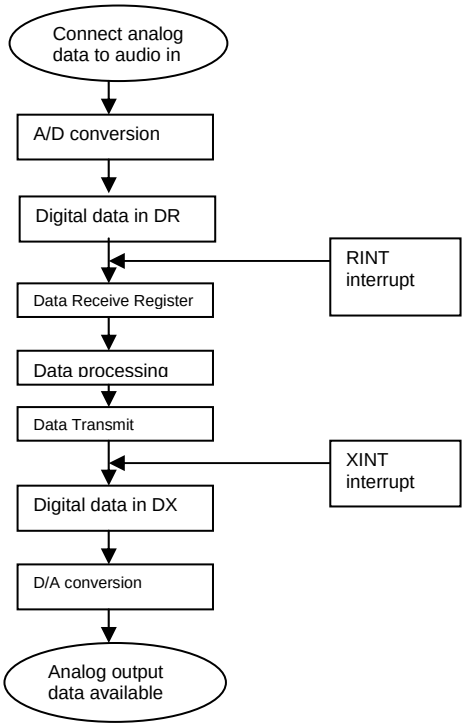

Fig.3 Flowchart of AIC.

3.1.2.1 Steps Of Analog Interface By AIC

1. Connect microphone with RCA audio in connector of CON7 of dsp kit.
2. Specific bit of TCR and SPC [6] is set in a C program for enabling data transfer and receive.
3. Then analog data is converted to digital data by a 14 bit A/D converter and available in DR pin . When IMR interrupt register is assigned value 10, RINT interrupt is asserted. Then data from DR is transferred to the Data Receive Register (DRR) via Receive Shift
4. Resister (RSR). DR to RSR transfer is serial but RSR to DRR transfer is parallel.
5. After processing received data it is assigned to data transmit register (DXR) [6]. When IMR is assigned 20 in a C program then XINT is asserted and data is transferred from DXR to DX pin via Transmit Shift Resister (XSR). DXR to XSR transfer is parallel but XSR to DX transfer is serial. Then digital data is converted to analog data by a 14 bit D/A converter. Following figure shows how serial port data receive and transfer occurs by XINT and RINT pulse [6].

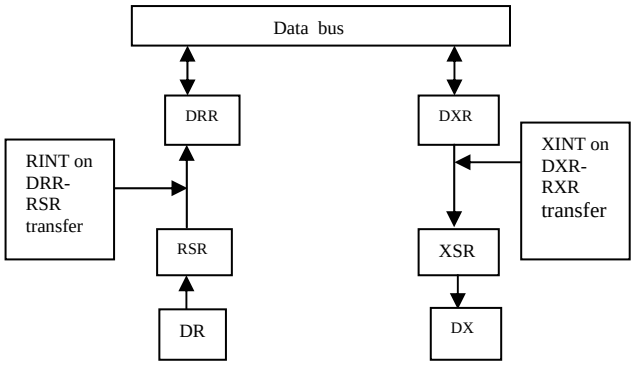

Fig.4 Process of data transfer by pulse.

4. Implementation Procedures

A simple CDMA system is implemented by TMS320C50 kit by following steps:
Step 1: Connect one microphone to the Audio In port of AIC and another to the pin 1 of A/D converter.
Step 2: For synchronization of taking two signals at a time both the signal are captured by executing rint() function. For default operation of AIC following DSP kit registers need to assign TCR = 0x0020 and PRD = 1 or more Here sampling frequency is 16 KHz if PRD = 1.
Captured voice signals looks like follows:

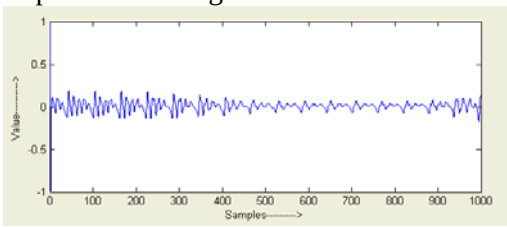

Fig.5 voice signal 1

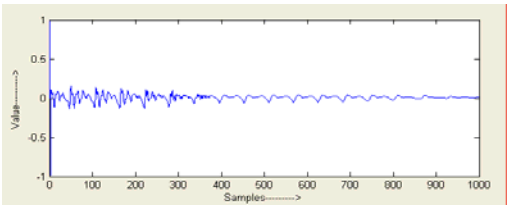

Fig.6 voice signal 2

Step 3: Two captured signal are spreaded by walsh code , added together and modulated by QPSK. CDMA system use 64 chip walsh code. After spreading spreaded signal looks like follows:

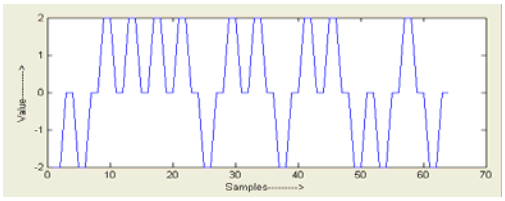

Fig.7 spreaded signal.

Step 4: If spreading and modulation take more time than interval between two successive sample , then for reducing sampling rate large value is assigned to the PRD register . For example maximum sampling rate is 19.6 KHz. So time needed for taking a sample is (1/19.6)ms or 50micro second. If Default sampling rate 16KHz is used then time between two sample is (1/16)ms or 62.5 micro second. So (62.5-50) = 12.5 micro second time is available to spread and modulation . If this time is not enough to spread and modulation then in side rint() function then large value is assigned to the PRD to reduce sampling frequency. This confirms real time implementation .

Step 5: At the receiver end signal is demodulated and pass to a low pass filter. And then despreaded by multiplying demodulated signal with walsh code.

Step 6: Then two signals are separated and voice signal is sent to the speaker through Audio Out port of AIC and other signal is sent to the oscilloscope through D/A converter.

5. Experimental Data And Analysis

Samples of captured input signals , spreading samples and modulated samples were displayed in the LCD display of kit. As resisters of kit is 16 bit, so 16 bit hexadecimal values were shown in the LCD display [6].

Among them only 16 samples of each type is listed in the following table-

Table 2: Resultant Input Samples, Spreading Samples, Modulated Samples Captured From Lcd Display.

First 16	First 16	First 16	First 16
0x0218	0xFD47	0xEC28	0x0430
0x0327	0xF93C	0xCD48	0x10F8
0x0023	0xF56C	0xD9C8	0x1BA0
0x0145	0xF220	0xD750	0x21B8
0x0213	0xEF60	0xDF08	0x2360
0x0411	0xF2D8	0xDB30	0x1F10
0x0067	0xF85C	0xE640	0x1620
0x1120	0xFCFC	0xDE50	0x09F8
0x0090	0x017C	0x0750	0xFC40
0xFF20	0x0578	0x31F8	0xEF20
0xFE45	0x0970	0x2690	0xE430
0xFCA2	0x0C9C	0x2838	0xDDB0
0xFF78	0x0FE8	0x2060	0xDB98
0x0193	0x0D8C	0x2418	0xDF40
0x0222	0x07E0	0x19A0	0xE7B8
0x0009	0x0340	0x2058	0xF360

Here two samples from two voice signals are taken at a time. First two samples are 0xFF20 and 0xFD47

So, $(FF20)_{16} = (1111111100100000)_2$ and $(FD47)_{16} = (1111110101000111)_2$

Starting bit of both the signals are 1. So this 1 is represented by corresponding 64 chip walsh code and summed together.

Spreading starting bit of Signal 1:

1 => 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Spreading starting bit of Signal 2:

1 => 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1

After summing two spreaded code:

2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0 2 0

In case of QPSK modulation all odd chips are 2 and all even chips are 0. So complex base band signal for sample 1 is (2 + j*0)

After spreading a sample, 64*16= 1024 chips are found. For QPSK modulation odd and even chips are separated to produce a complex base band signal for transmission.

Here it is clear that for transmitting a sample 1024 chips need to process. Sampling frequency of Taking samples are 8KHz . So interval between two samples are (1*1000000)/8000 =12.5 micro seconds. For real time processing all the 1024 chips need to process within 12.5 micro seconds. Because after this time another samples will appear. C coding of implementation doesn't take more time than 12.5 microseconds as Processor speed is 40 MHz. At the receiving end reverse procedure is applied and same hardware is used. So it ensures real time implementation of CDMA system.

6. Discussion

In implementation decoded signal is same as input signal. Implementation of CDMA system was real time in TMS320C50 DSP kit because it's clock rate is 40 MHz and sampling frequency of input signals was 16 KHz . So it is clear that processing speed of DSP kit is very much faster than sampling frequency that is the main key of real time implementation because after taking a sample value DSP processor get a lot of time for spreading and dispreading the signal. Here

spreading and de-spreading of signal is monitored in LCD display and oscilloscope.

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