Advanced Switching Sequences Based Model-Predictive Control for Single-Phase NPC Converters

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***Abstract*—This article presents a continuous control set model-predictive control (MPC) technique based on advanced switching sequences (SSs) for a grid-connected single-phase three-level neutral-point-clamped converter. The SSs are developed considering the tracking performance of the current feed to the utility grid, the dc-bus capacitor voltage balancing, and the switching loss of the semiconductor devices. In the proposed strategy, with the same sampling frequency, the number of pole state changes (SCs) per control cycle is only two, while in the optimal SS and the modulated MPC (pulse pattern similar to the conventional space vector modulation technique) schemes, the number of pole SCs is four. The reduction in the number switching SCs per control cycle considerably reduces the switching loss of semiconductor devices. Moreover, to avoid the challenges of utilizing the weighting factor, a single-objective cost function is adopted to track the reference current, and the dc-bus capacitor voltages are balanced using the redundancy nature of the voltage vectors. Furthermore, the proposed scheme can ensure a fixed-switching-frequency operation, which is advantageous for selecting filter parameters during real-life implementation. The effectiveness of the proposed strategy is validated by the results obtained from both the simulation in MATLAB/Simulink and the experiment carried out using a downscaled laboratory test rig.**

***Index Terms*—DC-bus voltage balancing, model-predictive control (MPC), single-phase multilevel converter, switching loss.**

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I. Introduction

RECENTLY, single-phase multilevel converters (MLCs) have attracted great attention because of their utilization in various fields, including the grid integration of distributed energy sources, railway electric traction, and electric vehicle charging systems [1], [2]. However, with the rising penetration in diverse application areas, their proper control has also become challenging.

Currently, the model-predictive control (MPC) technique has been emerged as one of the most dominant approaches to control grid-connected power converters because of its diverse usefulness, including straightforward implementation, ability to handle nonlinear constraints and different target variables, and robust dynamic characteristics [3], [4]. The standard finite-set model-predictive control (FS-MPC) technique [5], [6] considers the discrete-time system model and all the valid voltage vectors (VVs) of the converter to forecast the controlled variables at the next sampling instant. Then, the FS-MPC evaluates each of the VVs in a single- or multiobjective cost function to determine the system performance. The VV corresponding to the lowest cost function value is selected to be applied during the next control cycle. One of the major shortcomings of FS-PMC is that it operates at variable switching frequency with a distributed harmonics spectrum because a single VV is employed during the entire control cycle. Moreover, to preserve the current quality, the FS-MPC algorithm needs to be executed with a sampling rate, which should be high enough and greater than the desired switching frequency [7].

To address the challenges of FS-MPC, several techniques have been reported in the literature [8]–[10]. For instance, in [8], an improved FS-MPC, which guarantees constant switching frequency operation, is proposed for a single-phase T-type converter with a resistive–inductive load. The technique is, in fact, a single-objective modulated model-predictive control (M^2PC), where multiple VVs are utilized per control cycle with an inverse relationship between the vector dwell times and the respective cost functions. The technique uses a pulse pattern similar to the conventional space vector modulation (SVM) scheme to synthesize the converter output voltage. In [9], both single- and multiobjective-cost-function-based M^2PC strategies are investigated for a grid-connected three-phase three-level (3L) converter. Therein, the experimental results show that the

single-objective M^{2}PC technique exhibits improved performance than that of the multiobjective M^{2}PC technique in terms of the line current harmonic profile, the dc-bus voltage ripples, and the settling time during the power reference change. Moreover, the real-life implementation of the single-objective M^{2}PC technique is much easier due to the absence of a weighting factor.

To achieve a constant switching frequency operation, the discrete space vector modulation (DSVM) technique is proposed in [11]–[13], where a finite number of virtual VVs along with the real vectors of the converter are utilized to synthesize the converter output voltage. However, the DSVM technique suffers from computational overload because this strategy requires evaluating all the VVs per control cycle, the same as the FS-MPC scheme.

Another familiar strategy to produce a constant switching frequency is to use continuous control set MPC (CCS-MPC) [14], [15]. In [16], a CCS-MPC, based on four optimal switching sequences (OSSs), is proposed for a grid-connected single-phase 3L neutral-point-clamped (NPC) converter. The technique is denominated as OSS-MPC. The OSS-MPC adopts a single-objective cost function, where four switching sequences (SSs) are evaluated per control cycle to minimize the current tracking error. However, the technique does not consider the dc-bus voltage-balancing issue. Afterward, the OSS-MPC is extended in [17], addressing the dc-bus voltage-balancing issue in the system cost function as the second target variable. However, the number of SSs has been increased by four as compared to that of the single-objective OSS-MPC approach, while the technique needs to evaluate at least six SSs per control cycle. Moreover, the technique suffers from the challenges of using the weighting factor in the system cost function.

One of the challenging tasks of MPC is to equalize the voltages across the two series capacitors in the dc bus when it is implemented for MLCs such as NPC, active-neutral-point-clamped (ANPC), or T-type converters [18]. In the aforementioned single-objective M^{2}PC techniques [8], [9], the dc-bus voltage balancing is obtained by regulating the dwell times of the redundant vectors in each control cycle according to the dc-bus voltage imbalance factor. On the contrary, the multiobjective M^{2}PC strategy [9] considers the dc-bus voltage-balancing issue in the cost function along with a weighting factor to set priority between the two objectives. However, due to the inclusion of the weighting factor in the system cost function, both the steady-state and dynamic performances of the system degrade [9]. Furthermore, selecting an optimal weighting factor is not an easy task [19], [20].

Another most significant concern of the power converters is the power loss that occurs in semiconductor devices. Although the conduction loss remains almost constant for equal output power, the switching loss is highly dependent on the converter switching control techniques [21], [22]. One of the most critical disadvantages of the aforementioned OSS-MPC and the M^{2}PC strategies is the high switching loss of the semiconductor devices that occurs due to the higher rate of switching per control cycle. The unnecessary switching actions cause excessive power loss that further results in higher thermal stress, reduction of efficiency, and, in the long run, loss of converter active lifetime.

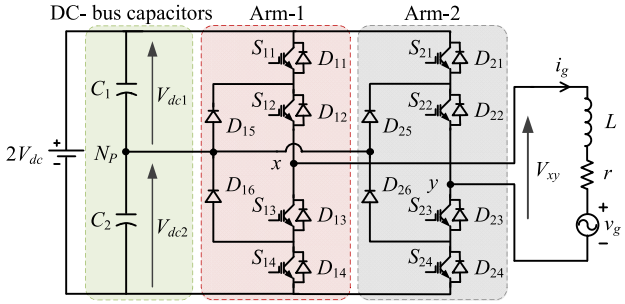

Fig. 1. Electrical structure of a single-phase 3L-NPC converter.

To address the aforementioned challenges, a CCS-MPC algorithm based on four advanced switching sequences (ASSs), which is denominated as ASS-MPC, is proposed in this article for the grid-connected single-phase 3L converters. Although the proposed scheme can be extended to other types of topologies such as T-type NPC and ANPC converters, only the basic principles are explained here for an NPC converter for easy and better understanding. The major outcomes of the proposed ASS-based MPC scheme are as follows.

1) In the proposed scheme, each of the SSs consists of two VVs, i.e., one zero or large VV and one of the two redundant small VVs. In each SS, the dwell time of the zero or large VV is split into two equal intervals and placed at the beginning and end of the SS, while one of the two redundant small VVs is placed at the middle position of the SS. As a consequence, a symmetrical pulse sequence is achieved, which results in an improved steady-state tracking and harmonic profile of the line current compared to that when dual-VV-based asymmetrical pulse sequence is used. Moreover, the total harmonic distortion (THD) of the line current under the proposed scheme is almost the same as that of the traditional single and multiobjective OSS-MPC schemes.
2) In the proposed technique, with the same sampling frequency, the number of pole state changes (SCs) per control cycle has been reduced by half compared to that of the traditional OSS-MPC and M^{2}PC schemes, resulting in a significant reduction (almost half) of the converter switching loss.
3) In the proposed scheme, the number of SSs to be evaluated per control cycle has been reduced to four from six compared to that of the multiobjective OSS-MPC scheme. Moreover, to eliminate the challenges of utilizing the weighting factor, a single-objective cost function is adopted to track the reference current. Furthermore, to achieve a solution to the dc-bus voltage-balancing problem, only one of the two redundant small vectors is selected per control cycle instead of employing both of the redundant vectors and regulating their dwell times.

II. Single-Phase 3L-NPC Converter

The electrical structure of a grid-connected single-phase 3L-NPC converter is shown in Fig. 1. $2V_{\rm dc}$ is the input dc voltage source, $V_{\rm dc1}$ and $V_{\rm dc2}$ represent the dc-bus voltages, C_1 and C_2

TABLE I
RELATIONSHIP AMONG THE IGBT STATE, POLE VOLTAGE, AND POLE STATE

S_{11}/S_{21}	S_{12}/S_{22}	S_{13}/S_{23}	S_{14}/S_{24}	V_{xNP}/V_{yNP}	Pole state
ON	ON	OFF	OFF	$+V_{dc}$	1
OFF	ON	ON	OFF	0	0
OFF	OFF	ON	ON	$-V_{dc}$	-1

TABLE II
VVS OF THE SINGLE-PHASE 3L-NPC CONVERTER

Voltage Vector, V_j	Pole 'x' state	Pole 'y' state	Output voltage, v_{xy}	N_p voltage (Inverter)	N_p voltage (Rectifier)
V_1	1	-1	$+2V_{dc}$	NE	NE
V_2	0	-1	$+V_{dc}$	D	I
V_3	-1	-1	0	NE	NE
V_4	1	0	$+V_{dc}$	I	D
V_5	0	0	0	NE	NE
V_6	-1	0	$-V_{dc}$	D	I
V_7	1	1	0	NE	NE
V_8	0	1	$-V_{dc}$	I	D
V_9	-1	1	$-2V_{dc}$	NE	NE

N.B: NE means no effect, D means decrease, and I means increase.

are the two series capacitors, and Arm-1 and Arm-2 are two insulated-gate bipolar transistor (IGBT) arms of the converter. Each of the arms contains four IGBTs and two clamping diodes. The relationships among the "ON" or "OFF" condition of the individual switches and pole voltages are presented in Table I. Since each of the poles can generate three different voltage levels, it is possible to generate $3^3 = 9$ different valid VVs for the converter. The available nine discrete VVs V_j with $j \in \{0, 1, \ldots, 9\}$ of the converter are summarized in Table II. Among these, there are three zero VVs, i.e., V_3, V_5, and V_7, four small VVs, i.e., V_2, V_4, V_6, and V_8, and two large VVs, i.e., V_1 and V_9. Each of the small VVs has one redundant vector. The redundant vectors can generate a same output voltage. However, they have opposite effects on the neutral point (N_P) potential. The zero and large VVs do not affect the N_P potential. Therefore, it is enough to consider the seven VVs $V_1, V_2, V_4, V_5, V_6, V_8$, and V_9 to produce the five different voltage levels, i.e., $0, +V_{\rm dc}, +2V_{\rm dc}, -V_{\rm dc}$, and $-2V_{\rm dc}$ and regulate the dc-bus capacitor voltages.

III. CONVENTIONAL CONTROL STRATEGIES

The single-objective OSS-MPC [16] considers four SSs to control the NPC converter. Each of the SSs contains three VVs, where there are two redundant small VVs and one zero or large VV. The zero or large VV is placed in the middle of two redundant small VVs. The dwell time of the small VV is divided equally between the two redundant VVs. The arrangements of the VVs for two arbitrary SSs of the single-objective OSS-MPC scheme are shown in Fig. 2(a), where the similar VVs are colored with the same color. From Fig. 2(a), it is clear that when the output voltage changes between two adjacent voltage levels, the total number of pole SCs per control cycle is four, which is equivalent to eight individual switching SC, as understood from Table I. This is also true for the other SSs.

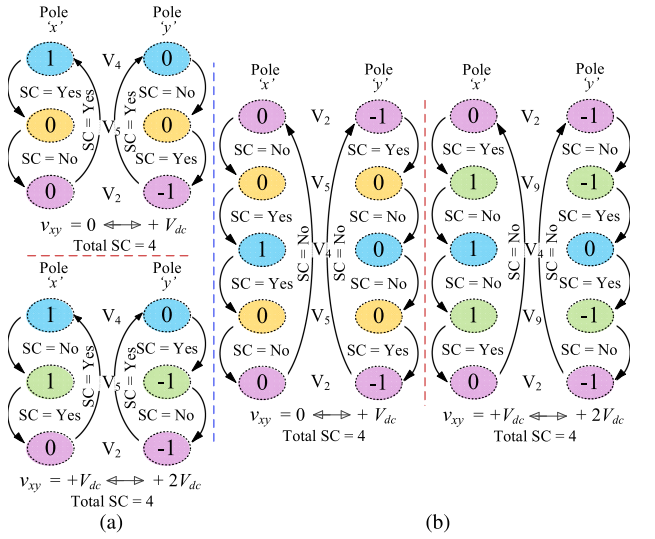

Fig. 2. Arrangements of the VVs and the respective pole SC for two SSs of (a) single- and multiobjective OSS-MPC schemes [16], [17] and (b) single- and multiobjective M^{2}PC schemes [8], [9].

The multiobjective OSS-MPC [17] considers eight optimal SSs. Among the eight SSs, four are similar to that of the single-objective OSS-MPC scheme. In these four SSs, the redundant small VVs have opposite effects on the N_P potential. On the contrary, the redundant small VVs of the other four SSs have similar effects on the N_P potential. However, in each of the SSs, the total number of pole SCs per control cycle is four.

A fixed-switching-frequency single-objective M^{2}PC algorithm is reported in [8] for a single-phase 3L T-type converter. The technique utilizes two VVs per control cycle, with an arrangement similar to that of the traditional SVM scheme. As a consequence, the line current ripples are greatly reduced. However, the switching losses of the semiconductor devices are significantly increased due to the extra switching operations per control cycle. For instance, when the M^{2}PC scheme adopts a pulse pattern similar to the SVM scheme, the total number of pole SCs per control cycle is four, as shown in Fig. 2(b).

IV. PROPOSED MPC ALGORITHM FOR SINGLE-PHASE 3L-NPC CONVERTER

A. System Mathematical Model

From Fig. 1, the dynamic response of the grid current in continuous time can be expressed as

$$di_g/dt = (v_{xy} - ri_g - v_g)(1/L) \tag{1}$$

where i_g and v_g denote the grid current and the grid voltage, respectively. L and r are the inductance and resistance of the line filter, respectively. Considering that the sampling period is very small compared to the system time constant, (1) can be synthesized in discrete time using the Euler method as

$$(i_g(k+1) - i_g(k))(L/T_s) = v_{xy}(k) - ri_g(k) - v_g(k) \tag{2}$$

where T_s is the control cycle or the sampling period. k and $k+1$ denote two consecutive control cycles. Since T_s is very small, v_g remains almost constant during the entire time of T_s. Therefore,

the rate of change of i_g during T_s is determined by v_{xy} and can be expressed as

$$f_j(v_{xy}) = (di_g/dt)|_{v_{xy}=V_j}, \quad j \in \{1\ldots.9\} \tag{3}$$

where $f_2 = f_4$, $f_6 = f_8$, and $f_3 = f_5 = f_7$. An SS S_m, which consists of two VVs of the converter, can be considered as

$$S_m = \{V_c, V_d\} \tag{4}$$

where $V_c, V_d \in \{V_1, \ldots, V_9\}$. The dwell times of the VVs V_c and V_d are t_c and t_d, respectively, where

$$t_c + t_d = T_s. \tag{5}$$

Using (3) and (4), the current at the end of T_s can be obtained from (6) as

$$i_g^p(k+1) = i_g(k) + f_{V_c} t_c + f_{V_d} t_d \tag{6}$$

where $i_g^p(k+1)$ and $i_g(k)$ stand for the predicted and the measured grid current at the moments $k+1$ and k, respectively. f_{V_c} and f_{V_d} denote the slope of i_g for the VVs V_c and V_d, respectively. When the SS S_m is applied, the respective current error at the moment $k+1$ can be expressed as

$$e_{i_g}(k+1) = i_g^r(k+1) - i_g^p(k+1) \tag{7}$$

where $i_g^r(k+1)$ is the reference current at the instant $k+1$, which can be obtained using the extrapolation theorem as

$$i_g^r(k+1) = 3i_g^r(k) - 3i_g^r(k-1) + i_g^r(k-2). \tag{8}$$

When the sampling frequency is very high, it can be assumed that the reference currents at the moment $k+1$ and k are equal, i.e., $i_g^r(k+1) = i_g^r(k)$. Taking into account (6), (7) results in

$$e_{i_g}(k+1) = i_g^r(k+1) - i_g(k) - f_{V_c} t_c - f_{V_d} t_d. \tag{9}$$

For the NPC converter, two target objectives are employed in the MPC algorithm. The first one is the exact current tracking and the second one is the N_p voltage balancing. Taking these two objectives into account, a cost function can be defined as follows:

$$g(k) = e_{i_g}^2(k+1) + \lambda e_{N_P}^2(k+1) \tag{10}$$

where $e_{N_P}(k+1)$ stands for the N_P voltage-balancing error at the moment $k+1$ and λ is the weighting factor for N_p voltage balancing. In the proposed algorithm, the N_p voltage balancing is achieved by using the redundancy characteristics of the small VVs, which is discussed in Section IV-D. Consequently, the cost function of the proposed ASS-MPC algorithm is reduced to

$$g(k) = e_{i_g}^2(k+1). \tag{11}$$

Equation (11) indicates that the cost function of the proposed technique is single-objective, in which only the current tracking error is considered. From (2), it is clear that the current trajectory depends on the output voltage levels, not on the effects of the VVs on the N_P potential. As a consequence, the proposed strategy needs to evaluate only five voltage levels per control cycle. To calculate the dwell times of the VVs in S_m that will minimize the system cost function $g(k)$ value, the partial

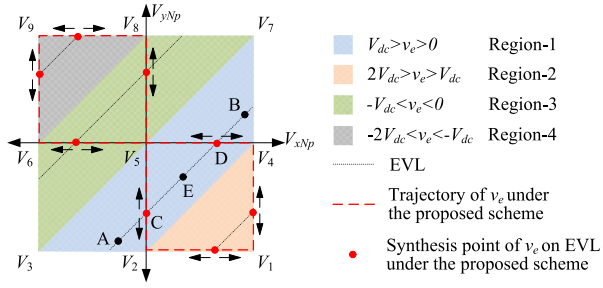

Fig. 3. Control area of single-phase 3L-NPC converter with feasible VVs and probable solutions to constitute v_e.

derivatives of $g(k)$ with respect to t_c and t_d are set to zero as the following equations:

$$\partial g(t_c, t_d)/\partial t_c = 0, \quad \partial g(t_c, t_d)/\partial t_d = 0. \tag{12}$$

Solving (12), the values of t_c and t_d can be obtained as

$$\begin{cases} t_c = \frac{i_g^r(k+1) - i_g(k) - f_{V_d} T_s}{f_{V_c} - f_{V_d}}, & 0 \le t_c \le T_s \\ t_d = T_s - t_c, & 0 \le t_d \le T_s \end{cases}. \tag{13}$$

Therefore, for the VV set $\{v_c, v_d\}$ of S_m, the optimal dwell time set is $\{t_c, t_d\}$. Then, the value of $g(k)$ for $\{v_c, v_d\}$ can be calculated using (11). Similarly, the optimal dwell time sets and the respective cost function values for the other SSs can also be calculated. Finally, the SS corresponding to the minimum cost function value is selected as the best SS S_{best}. Therefore, S_{best} can be defined as

$$S_{\text{best}} = \arg \left\{ \min_{\text{All SSs}} \{g\} \right\} \tag{14}$$

with the respective best time set T_{best} and the best VV set V_{best} as

$$V_{\text{best}} = \{V_c', V_d'\} \quad \text{and} \quad T_{\text{best}} = \{t_1, t_2\}. \tag{15}$$

Once V_{best} and T_{best} are determined, then an equivalent voltage v_e can be calculated using the volt–second balance principle. It can be defined as

$$v_e = (V_c' t_1 + V_d' t_2)/T_s. \tag{16}$$

B. Selection of Suitable Synthesis Point to Constitute v_e

According to (14), a proper number of SSs are required to be tested for the purpose of selecting the best one. These SSs can be defined taking into account the discrete characteristics of the VVs of the NPC converter. The nine available VVs of the NPC converter are plotted in Fig. 3. The entire control area covered by these VVs can be divided into four regions depending on the magnitude of v_e, which is also shown in Fig. 3.

In each of these regions, a line with equal average output voltage, which is defined here as equal voltage line (EVL), can be considered [23]. In a particular region, v_e can be synthesized into a number of VVs depending on the position of v_e on the EVL. For example, when v_e is assumed to locate at point E in region 1, the VV set $\{V_4, V_5, V_2\}$ is needed to synthesize v_e. On the contrary, if v_e is assumed to locate at point C or D, the VV set

TABLE III
SSs OF THE PROPOSED SCHEME

Region	Switching sequence	Voltage vector sequence	Comments	Output PWM voltage
1	S_1	$\{\underbrace{V_5}_{t_1/2}, \underbrace{V_a}_{t_2}, \underbrace{V_5}_{t_1/2}\}$	$V_a = V_4$ or V_2	$0 \leftrightarrow +V_{dc}$
2	S_2	$\{\underbrace{V_1}_{t_1/2}, \underbrace{V_a}_{t_2}, \underbrace{V_1}_{t_1/2}\}$	$V_a = V_4$ or V_2	$+V_{dc} \leftrightarrow +2V_{dc}$
3	S_3	$\{\underbrace{V_5}_{t_1/2}, \underbrace{V_b}_{t_2}, \underbrace{V_5}_{t_1/2}\}$	$V_b = V_8$ or V_6	$0 \leftrightarrow -V_{dc}$
4	S_4	$\{\underbrace{V_9}_{t_1/2}, \underbrace{V_b}_{t_2}, \underbrace{V_9}_{t_1/2}\}$	$V_b = V_8$ or V_6	$-V_{dc} \leftrightarrow -2V_{dc}$

$\{V_5, V_2\}$ or $\{V_5, V_4\}$, respectively, is required to synthesize v_e. For the assumption of v_e at point A or B, the VV set $\{V_2, V_5, V_6\}$ or $\{V_4, V_5, V_8\}$, respectively, is needed to constitute v_e. In the similar way, the VV sets to constitute v_e in other regions can also be decided from Fig. 3. Therefore, it may be concluded that the VVs $V_1, V_2, V_4, V_5, V_6, V_8$, and V_9 are sufficient to constitute v_e to its entire range.

In case of points A, E, and B, the minimum switching condition between two consecutive control cycles is violated, while for points C and D, the condition is reserved. Therefore, in regions 1 and 3, the intersection points between the EVL and the V_{xN_P} or V_{yN_P} line and in case of regions 2 and 4, the two extreme points on the EVL can be chosen as the desired synthesis points, which are marked as red dots, as shown in Fig. 3. Although the EVLs in every region contain two desired synthesis points, only one of them can be selected in a control cycle based on the N_P voltage condition. The red-colored dashed lines in Fig. 3 denote the trajectory of v_e under the proposed scheme.

C. Proposed SSs for the 3L-NPC Converter

In align with the analysis in Section IV-B, in total, four SSs are introduced for the proposed MPC algorithm approach. The proposed SSs along with their respective VVs and sequences are presented in Table III.

The variables in the underbrace of the VVs denote the activation time duration of those respective VVs. The VVs and their respective operation sequence in an SS are specified taking into account two factors. The first one is to minimize the line current ripple and the second one is to minimize the switching loss. Merging the concept of using multiple VVs to minimize the current ripple, in each SS, two VVs, including one zero or large VV and one of the two redundant small VVs, are employed such that the output voltage changes between two adjacent voltage levels.

Once the VVs for the SSs are specified, the next task is to determine their operation sequence. Although the volt–second average value over a control cycle is not affected by the position of the vectors, it greatly affects the harmonics and the tracking performance of the line current [24]. This can be explained from Figs. 4 and 5, which show two possible cases of VV placement for the SS S_2 when t_1 or $t_2 \neq 0$.

In the first case, the large VV V_1 is split into two equal intervals and placed at the beginning and end of the SS with the small VV

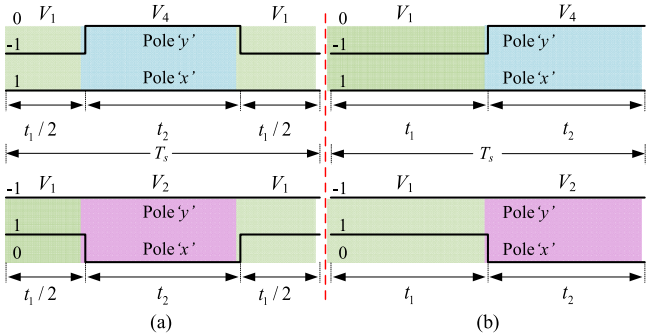

Fig. 4. Dual-VV-based (a) proposed symmetrical pulse sequence and (b) asymmetrical pulse sequence for the SS S_2.

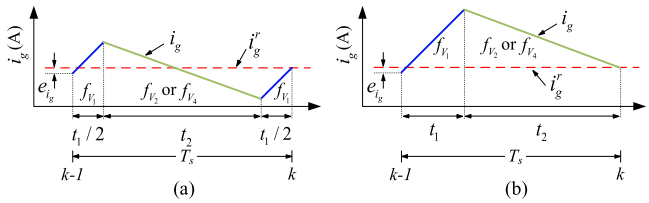

Fig. 5. Predicted current trajectory for the SS S_2 with (a) the proposed symmetrical pulse sequence and (b) asymmetrical pulse sequence.

V_4 or V_2 at the middle position that leads to a symmetrical pulse sequence in a control cycle. In the second case, the respective VVs are placed sequentially without any segmentation that leads to an asymmetrical pulse sequence. Moreover, although the values of i_g^p in both of the cases are equal at the end of T_s, the maximum deviation of i_g^p from i_g^r in the first case is less than that of the second case, as clearly understood from Fig. 5. Consequently, better performances in terms of steady-state line current tracking and the harmonic spectrum are achieved in the proposed dual-VV-based symmetrical pulse sequence method. Similar concepts for creating symmetrical pulse pattern have been explored in the literature [25]–[27] for various applications, including high-frequency link rectifier and dual-inverter-driven induction motor.

It should be noted that the small VVs are placed at the middle position of the SSs in order to avoid additional switching during the transition between two consecutive control cycles under the same region.

The total number of pole SC per control cycle for any of the SSs is equal to two, and it does not depend on the type of selected small VV, as can be clearly seen from Figs. 6 and 7. Furthermore, since the small VVs are placed at the middle position of the SSs, no SC occurs during the transition between two consecutive control cycles under the same region, no matter whether the selected small VVs are identical or distinct. For instance, the SS S_1 consists of the zero VV V_5 and the small VV V_4 or V_2. The possible two VV sequences are $V_5 - V_4 - V_5$ and $V_5 - V_2 - V_5$. In these two SSs, the total number of pole SCs in a control cycle is two. Since both of these SSs start and end with the VV V_5, no SC occurs during the transition between them, whatsoever the small VV is V_4 or V_2, as can be realized from the top-left most two subfigures of Figs. 6 and 7.

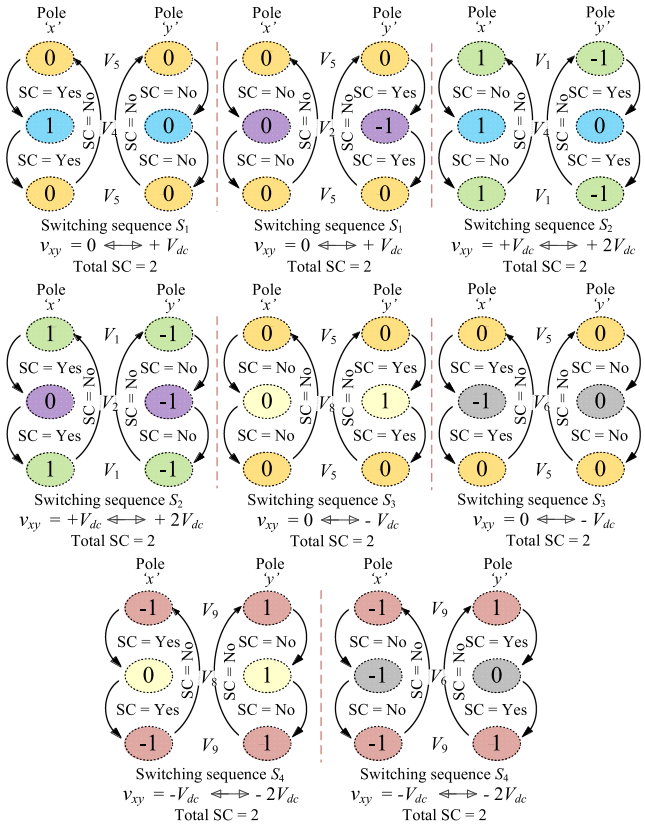

Fig. 6. VV sequences and the respective pole SC of the proposed ASS-MPC scheme when the selected small VVs in consecutive two control cycles are identical under the same region.

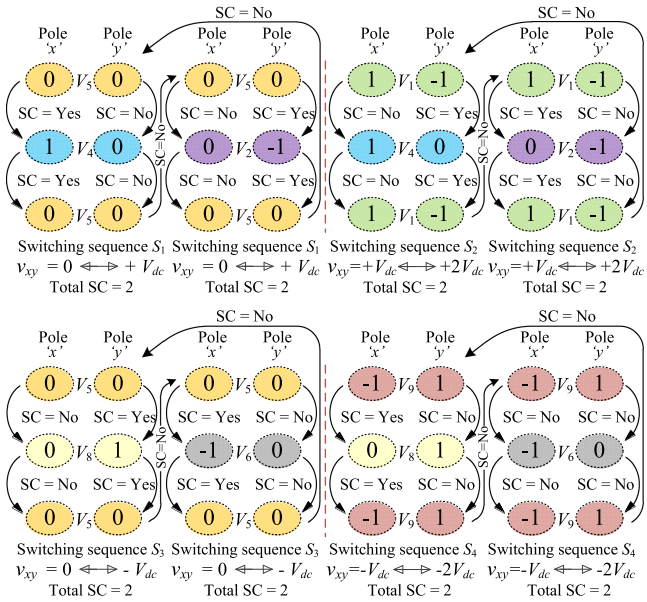

Fig. 7. VV sequences and the respective pole SC of the proposed ASS-MPC scheme when the selected small VVs in consecutive two control cycles are distinct under the same region.

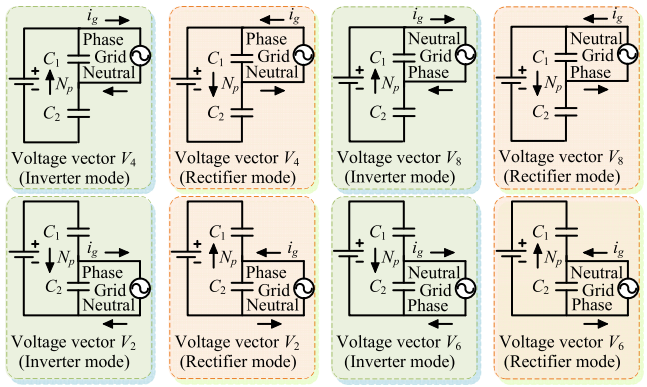

Fig. 8. Effects of small VVs on the N_P voltage.

D. N_P Voltage-Balancing Strategy

The dc-bus voltage imbalance $\Delta V_{\rm dc}$ is defined as the difference between the top capacitor voltage $V_{\rm dc1}$ and the bottom capacitor voltage $V_{\rm dc2}$ and is denoted as

$$\Delta V_{\rm dc} = V_{\rm dc1} - V_{\rm dc2}. \tag{17}$$

Once $S_{\rm best}$ along with the respective VV sequence and their optimal dwell times are determined, the next task is to select the correct small VV for $S_{\rm best}$ in order to achieve balanced N_P voltage. It is to be mentioned that there are two couple of redundant small VV sets $\{V_8, V_6\}$ and $\{V_4, V_2\}$, where the voltage generated by the first and second couples of VV sets are $+V_{\rm dc}, -V_{\rm dc}$, respectively. Since the VVs in each of the sets can generate same voltage, selecting one of them does not affect the current tracking performance. However, their effects on the N_P voltage are opposite [28], [29]. For a particular small VV, the N_P voltage will rise or drop depending on the direction of current at the N_P. The N_P voltage rises when the current enters into N_P and *vice versa*.

The direction of current at N_P is determined by two factors: first one is which capacitor is connected with the output load and the second one is the direction of power flow. For instance, when the VV V_4 is selected for the SS S_1 or S_2, the grid phase and neutral terminals are connected to the positive bus and N_P, respectively, as shown in the top-left most subfigure of Fig. 8. Under this situation, when the power flows from the converter to the grid (inverter mode of operation, $v_e i_g > 0$), the line current enters into N_P. In a consequence, the N_p voltage will increase, as depicted in the top-left subfigure of Fig. 8. On the contrary, when the power flows from the grid to the converter (rectifier mode of operation, $v_e i_g < 0$), the line current leaves from N_P and the N_p voltage will decrease. In a similar way, the effects of the other small VVs on the N_P voltage depending on the converter operation mode are presented in Fig. 8. The upward and the downward arrow at the N_P denote the voltage rise and voltage drop of N_P, respectively. The selection criterion of a particular small VV for an SS is summarized in Table IV.

TABLE IV
SMALL VV SELECTION TO BALANCE THE DC-BUS CAPACITOR VOLTAGES

Voltage vectors	Selected vector with condition
$\{V_5, V_a, V_5\}$	if ($V_{dc1} > V_{dc2}$ and $v_e i_g > 0$) or ($V_{dc1} < V_{dc2}$ and $v_e i_g < 0$)
$\{V_1, V_a, V_1\}$	$V_a = V_4$ and $V_b = V_8$,
$\{V_5, V_b, V_5\}$	else
$\{V_9, V_b, V_9\}$	$V_a = V_2$ and $V_b = V_6$

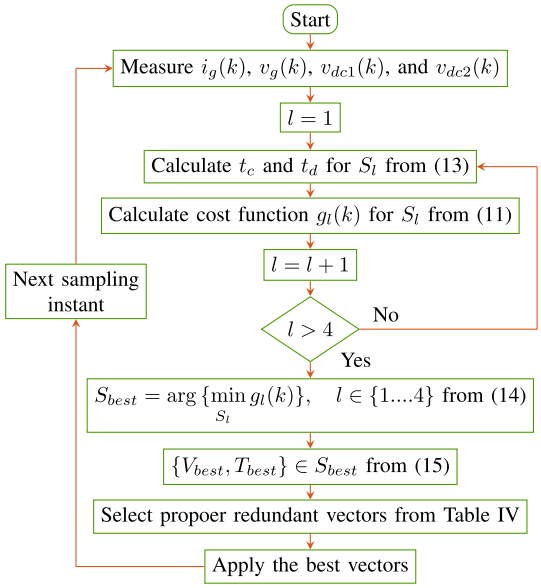

Fig. 9. Flowchart for the implementation of the proposed ASS-MPC algorithm.

TABLE V
SIMULATED AND EXPERIMENTAL PARAMETERS

Parameter	Symbol	Simulation	Experiment
Inverter rating	-	10 kVA	2 kVA
Grid voltage	v_g	230 V (50 Hz)	230 V (50 Hz)
DC-bus voltage	V_{dc}	400 V	400 V
DC-bus capacitors	C_1, C_2	4000 µF	2000 µF
Line filter	L, r	2 mH + 0.01 Ω	5 mH + 0.01 Ω
Sampling frequency	-	10 kHz	10 kHz

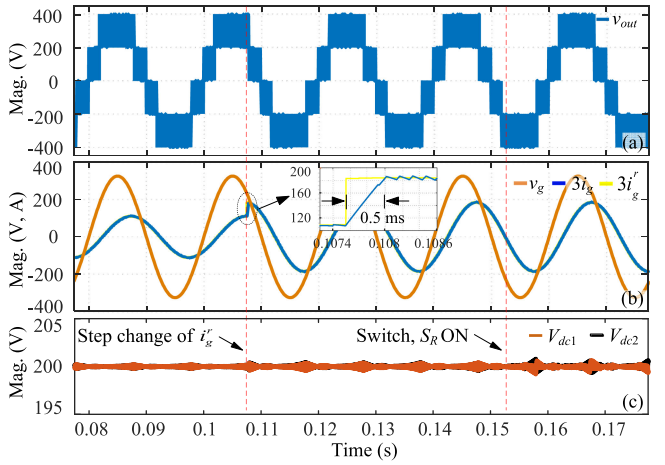

Fig. 10. Simulated waveforms to evaluate the steady-state, dynamic, and N_P voltage-balancing performance of the proposed ASS-MPC scheme. (a) Output voltage. (b) Line current. (c) DC-bus voltages.

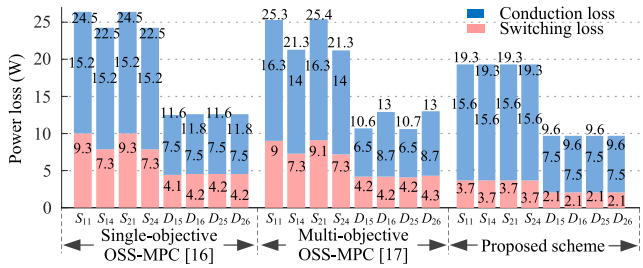

Fig. 11. Comparison of switching and conduction losses of IGBTs and diodes under various schemes.

Hence, from the above discussion, it can be concluded that the dc-bus N_P voltage can be balanced by proper selection of the small VV based on the magnitude $V_{\rm dc1}$ and $V_{\rm dc2}$ and the power flow direction without affecting the current tracking performance of the converter. The flowchart of the proposed ASS-MPC scheme is shown in Fig. 9. During practical implementation, the time delay caused by the processor is balanced by two-step forward prediction of the line current [30].

V. SIMULATION AND EXPERIMENTAL ANALYSIS

The feasibility of the proposed ASS-MPC scheme is verified with the results obtained from both the simulation and a reduced-scale laboratory test platform. The various simulation and experimental parameters of the case studies are mentioned in Table V. The parameters from the datasheets of Infineon IGBT/diode module F3L100R07W2E3_B11 are used in PLECS to obtain the power losses of the converter.

A. Simulation Results

The steady-state and dynamic performances of the proposed ASS-MPC scheme in terms of the output voltage, the line current, and the dc-bus voltages are presented in Fig. 10. In the proposed scheme, the converter can generate five-level line voltage as expected, which is shown in Fig. 10(a). Initially, input reference is set to operate the converter at 60% of the rated condition with 0.75 lagging power factor (pf). At an instant, a step change is made to the input reference to operate the converter at full rated condition. The converter can successfully track the reference current within 0.5 ms, as depicted in Fig. 10(b). Since in each control cycle, the small VV is selected based on the N_P voltage, the dc-bus capacitor voltages are balanced at 200 V without any significant ripples under both at steady-state and dynamic conditions, as shown in Fig. 10(c).

To further prove the dc-bus voltage-balancing ability of the proposed ASS-MPC scheme, a resistance R (100 Ω) is inserted across the lower capacitor of the dc bus, where a switch S_R is connected in series with the resistance. S_R is closed at an instant to force the dc-bus voltages to become unbalanced. However, the proposed scheme can maintain the normal operation of the converter in terms of the output voltage and tracking the reference current without any significant unbalance of the dc-bus voltages, as shown in Fig. 10(c).

The power losses in switches S_{11}, S_{14}, S_{21}, and S_{24} and diodes D_{15}, D_{16}, D_{25}, and D_{26} at full rated load and unity pf conditions under the various schemes are compared from Figs. 11–13. Under the single-objective OSS-MPC, the multiobjective OSS-MPC, the single-objective M^{2}PC, and the multiobjective M^{2}PC schemes, the total conduction losses are 183, 183, 183.4, and 184 W, respectively. Under these schemes, the total switching losses are 50, 50, 47, and 47 W, respectively. On

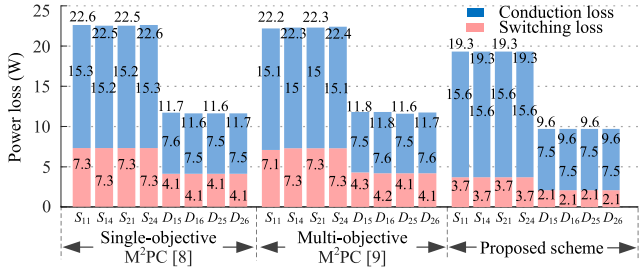

Fig. 12. Comparison of switching and conduction losses of switches and diodes under various schemes.

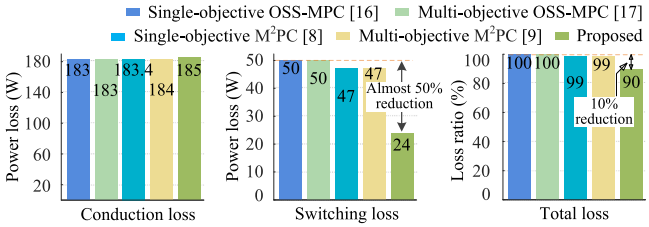

Fig. 13. Total power loss comparison of various schemes.

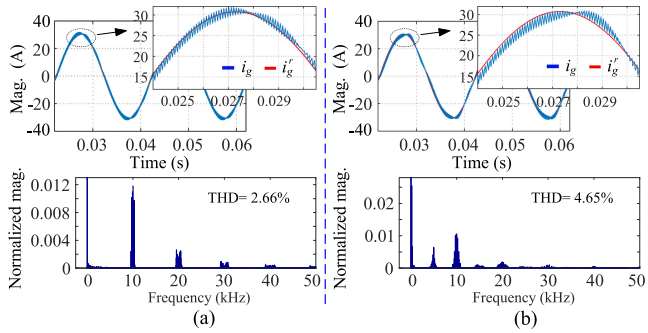

Fig. 14. Converter line current waveforms and the respective harmonics spectrum (a) under the proposed ASS-MPC scheme (with symmetrical SSs) and (b) with asymmetrical SSs.

the contrary, under the proposed technique, the total switching and the total conduction losses are 185 and 24 W, respectively, as shown in the first and second subfigures of Fig. 13, respectively. Under the proposed technique, the total conduction loss remains almost the same as that of the existing aforementioned techniques. In contrast, the total switching loss gets reduced by almost 50% as expected. This significant diminishing of switching loss is due to the reduction in the number individual switching SCs per control cycle when compared with the other traditional techniques. The reduction in the total loss in the converter is almost 10%.

To further verify the superiority of the proposed scheme, the line current waveforms along with the respective harmonic profiles at half rated load and 0.75 lagging pf conditions are investigated, as presented in Fig. 14(a). From Fig. 14(a), it can be seen that when the proposed technique is applied, an almost pure sinusoidal line current with good tracking performance is obtained. The high-frequency harmonic contents of the line current localize on the 10, 20, 30 kHz, etc., which are multiple of the sampling frequency. This facilitates some advantages to model the filter during the practical implementation. The

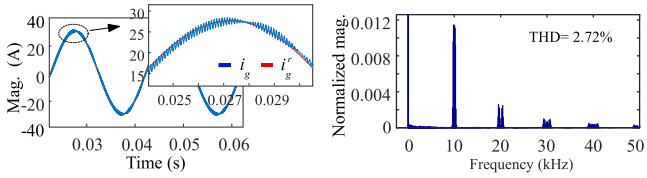

Fig. 15. Converter line current waveform and the respective harmonics spectrum under the single-objective OSS-MPC scheme [16].

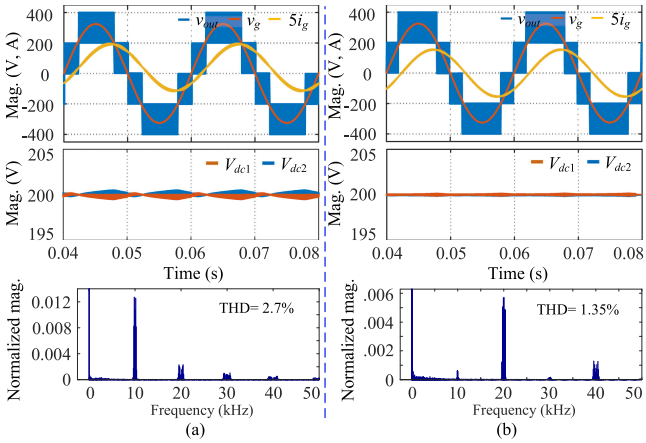

Fig. 16. Steady-state simulated waveforms and the respective line current harmonics spectrum of (a) the multiobjective OSS-MPC scheme [17] and (b) the single-objective M²PC scheme [8].

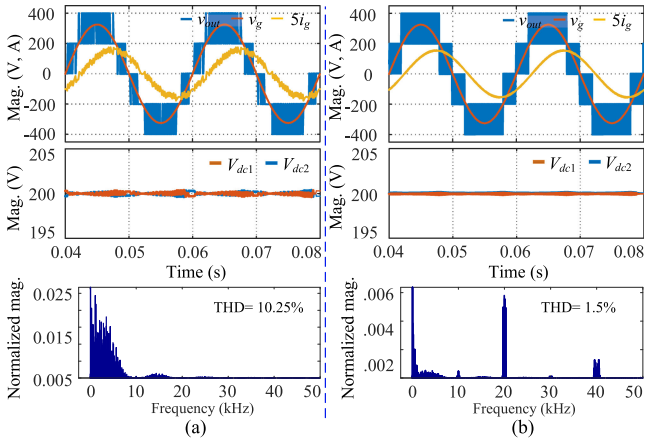

Fig. 17. Steady-state simulated waveforms and the respective line current harmonics spectrum of (a) the conventional FS-MPC scheme and (b) the multiobjective M²PC scheme.

obtained THD under the proposed scheme is 2.66%, which is much lower compared to that when the SSs having two VVs with asymmetrical pulse pattern are applied, as shown in Fig. 14(b). Moreover, the steady-state current tracking performance of the proposed technique is better than that of the asymmetrical pulse pattern. Fig. 15 shows the current THD (2.72%) under the single-objective OSS-MPC scheme, which is almost the same as that of the proposed ASS-MPC scheme.

The steady-state performance of the multiobjective OSS-MPC, the single-objective M²PC, the conventional FS-MPC, and the multiobjective M²PC schemes at half rated load and 0.75 lagging pf conditions is presented in Figs. 16(a), 16(b), 17(a), and 17(b), respectively. Each of the schemes can successfully

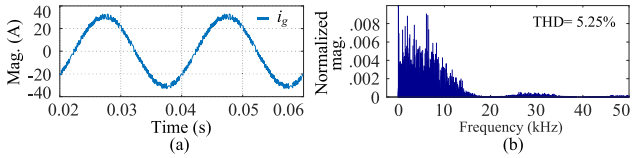

Fig. 18. (a) Steady-state simulated line current waveform and (b) the respective harmonics spectrum of the conventional FS-MPC scheme ($T_s = 50$ μs).

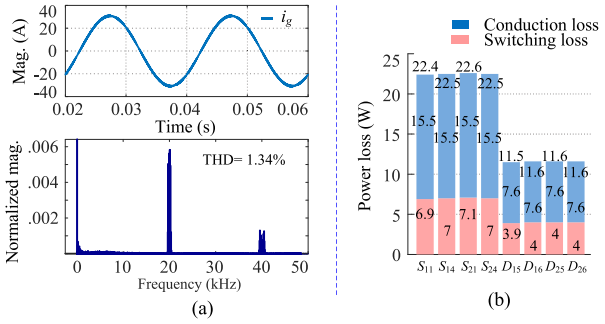

Fig. 19. (a) Converter line current waveform and the respective harmonics spectrum and (b) power losses under the proposed scheme ($T_s = 50$ μs).

balance the dc-bus voltages. The line current THDs under these schemes are 2.7%, 1.35%, 10.25%, and 1.5%, respectively. The current THDs of the single- and multiobjective M^{2}PC schemes are better than that of the proposed ASS-MPC scheme. However, the total switching loss under these schemes is almost double than that of the proposed technique. Moreover, the line current THD (2.66%) under the proposed technique is still under the acceptable range.

The conventional FS-MPC is simulated for different sampling frequencies, and the respective average switching frequencies are calculated. It is found that when the FS-MPC sampling frequency is set to 20 kHz, the respective average switching frequency becomes equal to that of the proposed ASS-MPC technique. Fig. 18 shows the simulated results of the FS-MPC scheme with the same average switching frequency as that of the proposed scheme. Moreover, Fig. 18 shows that current THD of the FS-MPC scheme (5.25%) is much higher than that of the proposed scheme (2.66%).

For fair comparison, the proposed technique is compared with the single- and multiobjective M^{2}PC schemes based on equal number of switching SCs per control cycle. To do so, the proposed scheme is simulated with 20-kHz sampling frequency, and the respective results are shown in Fig. 19, from where it can be seen that the power losses and the current THD are almost the same as that of the single-objective M^{2}PC scheme. However, the current THD (1.34%) is still better than that of the multiobjective M^{2}PC scheme (1.5%).

The dc-bus voltage-balancing ability of the proposed scheme with unequal split capacitor values ($C_1 = 4000$ μF and $C_2 = 2000$ μF) is much better than that of the single-objective M^{2}PC scheme, as presented in Fig. 20. From Fig. 20, it can be seen that the single-objective M^{2}PC scheme needs more than 0.4 s to balance the dc-bus voltages with $\Delta V_{\rm dc} = 1.5$ V. The technique uses both of the two redundant vectors per control cycle and

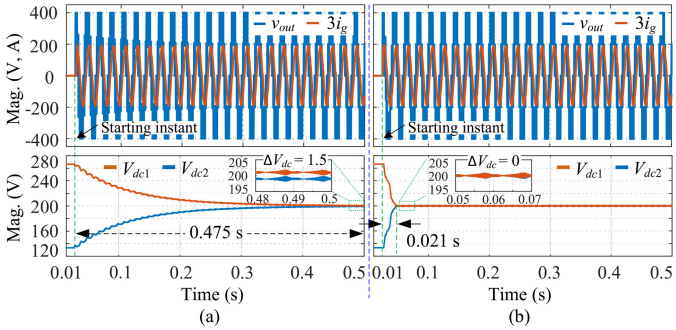

Fig. 20. Comparison of N_P voltage-balancing ability with unequal dc-link capacitor values. (a) Single-objective M^{2}PC scheme. (b) Proposed ASS-MPC scheme.

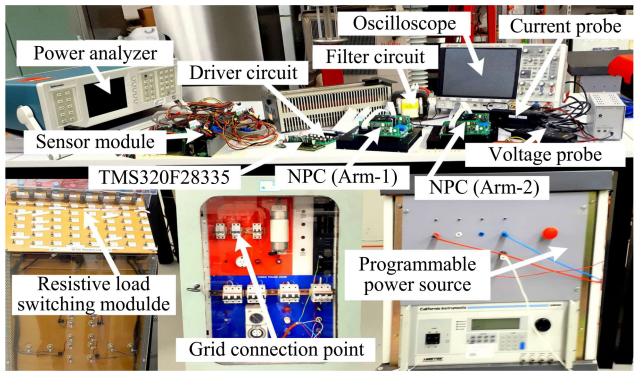

Fig. 21. Photograph of the experimental test rig.

regulate their dwell times in accordance to the N_P voltage unbalance factor. Consequently, the technique requires a long time to balance the dc-bus voltages. In contrast, the proposed technique can balance the dc-bus voltages within 0.021 s with $\Delta V_{\rm dc} = 0$ V. This fast balancing is due to the use of only one of the two redundant vectors per control cycle. The performance comparison of various techniques is presented in Table VI.

B. Experimental Results

To test the excellency of the proposed ASS-MPC technique, a 2-kVA laboratory test rig has been implemented, as shown in Fig. 21. The two legs of the NPC converter are constructed with IRG4PH40UPbF IGBTs and IDH15S120 diodes from Infineon. The proposed algorithm is programmed in the TMS320F28335 processor from the Texas instruments. The grid coupling point and the 5.5-kVA 312-V AMETEK CSW5550 power supply module are shown in Fig. 21. To test the dc-bus voltage-balancing ability, a resistive load (100 Ω) switching module is connected for the intentional switching of S_R.

Fig. 22 shows the steady-state and transient performances of the proposed ASS-MPC scheme. Fig. 22(a) shows the PWM output voltage when the proposed technique is applied, with the corresponding grid voltage and grid current waveforms. At the starting, S_R is kept disconnected and the NPC converter is operated at 50% rated condition with 0.75 lagging pf. The dc-bus voltages are perfectly balanced to 200 V. The zoomed

TABLE VI
PERFORMANCE COMPARISON FOR DIFFERENT TECHNIQUES

Ref.	Number of SS	Number of SS required to test in T_s	Number of pole SC in T_s	Switching loss	N_P voltage balancing	Weighting factor	Computational complexity	THD at steady-state condition
[16]	4	4	4	More	Not considered	-	Less than [17]	Moderate
[17]	8	6	4	Same to [16]	Considered	Yes	More	Almost same to [16]
Proposed	4	4	2	Almost half of [16], [17]	Considered	No	Less than [17]	Almost same to [16]

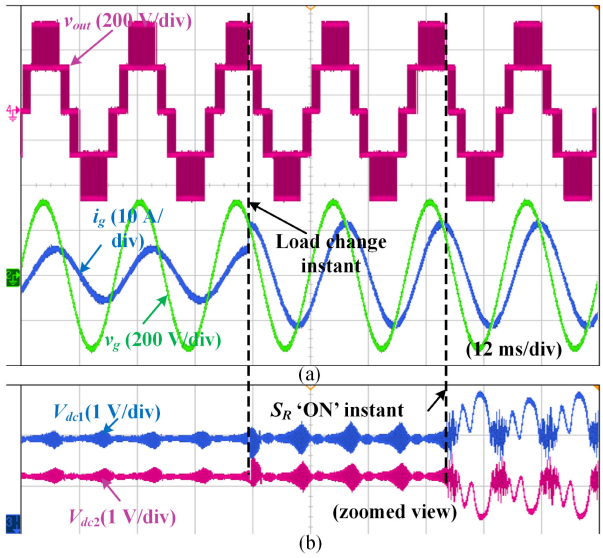

Fig. 22. Steady-state and dynamic performance of the NPC converter with the proposed ASS-MPC scheme. (a) Output PWM voltage, grid current, and grid voltage. (b) Zoomed view of the dc-bus voltages.

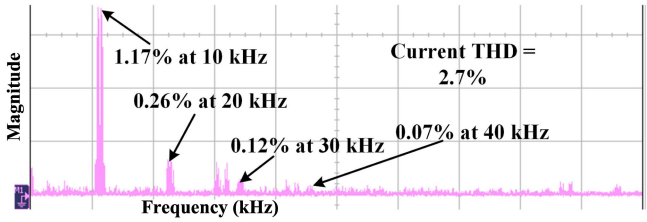

Fig. 23. Line current harmonics under the proposed ASS-MPC scheme.

view of the voltages are illustrated in Fig. 22(b) to demonstrate the negligible voltage ripples.

At an instant, a step change is made in the reference current to operate the converter in full rated condition. This instant is termed as load change instant in Fig. 22(a). The grid current keeps tracking the reference within 0.65 ms, ensuring very fast control dynamics. As the current is now increased, the dc-bus voltage ripples are also increased. However, they are less than 1 V. To test the stability of the proposed scheme, at an instant, S_R is turned "ON" and termed as S_R "ON" instant in Fig. 22(b). Fig. 22(a) shows that the grid voltage and current are not affected, and the proposed MPC algorithm can strictly balance the dc-bus voltages, as shown in Fig. 22(b). Although ripples are increased, they remain within 1.5 V and can be considered insignificant. Fig. 23 shows the experimental harmonic spectra of the line current with a THD of 2.7%, where the harmonic contents are

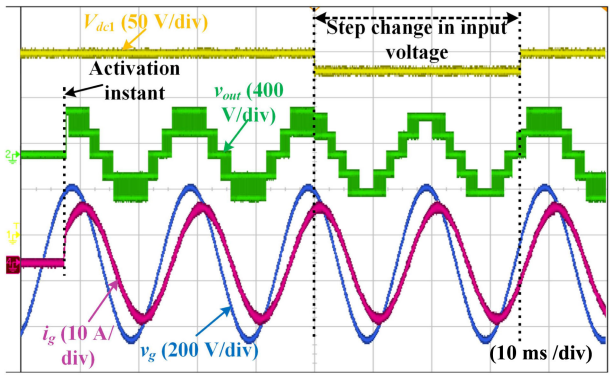

Fig. 24. Performance of the proposed ASS-MPC scheme during the start-up instant and the input dc voltage variations.

expressed as the percentage of the fundamental component of the line current. The oscilloscope fast Fourier transform window is operated in "Hanning" mode for the acquisition of the spectra. The efficiency of the converter is also improved, as the proposed method does not require double-switching-frequency operation per control cycle. Therefore, switching losses are reduced, as already shown in Fig. 13. The efficiency is measured with the PA4000 power analyzer from Tektronix. The efficiency is found to be around 98.2% at the rated load. It is to be noted that the power losses in the filter circuit, the biasing circuit, and the driver circuit are omitted.

Fig. 24 shows the start-up and the input dc voltage variation responses of the converter when the proposed control technique is applied. Initially, the converter remains in "OFF" state. At a particular instant, the proposed control algorithm is activated and the converter starts smoothly. Then, at a particular moment, a manual variation followed by a step change is made to the input dc voltage to decrease it from 400 to 350 V. After a short duration of time, action is taken to recover the dc voltage to its original value. From Fig. 24, it can be seen that the converter exhibits excellent performance with the sudden input dc voltage variations without any significant distortion in the line current.

The experimental steady-state results of the multiobjective FS-MPC scheme are shown in Fig. 25. The scheme can balance the dc-bus voltages with a ripple of around 3 V. However, the line current shows high ripple with a THD of 10.73%.

The experimental steady-state waveforms of the OSS-MPC scheme with 5-kHz sampling frequency are presented in Fig. 26. The experiment is carried out based on equal number of switching SCs per control cycle, the same as that of the proposed ASS-MPC scheme. The dc-bus voltage ripples are found to be

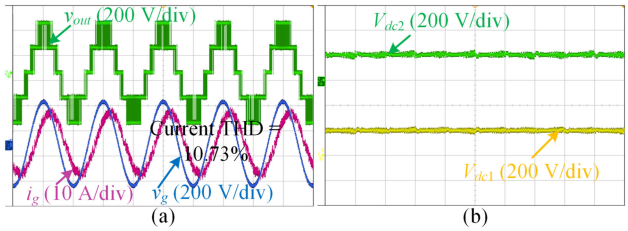

Fig. 25. Steady-state performance of the conventional FS-MPC scheme. (a) Output voltage and line current. (b) DC-bus voltages.

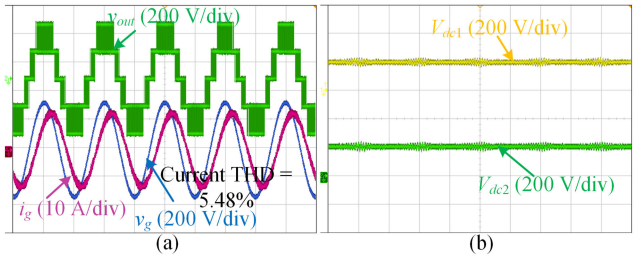

Fig. 26. Steady-state performance of the OSS-MPC scheme. (a) Output voltage and line current. (b) DC-bus voltages ($T_s = 200$ μs).

around 4 V. The experimental line current THD is found to be 5.48%, which is much higher than that of the proposed scheme.

VI. Conclusion

In this article, an ASS-MPC algorithm was presented for a grid-connected single-phase 3L-NPC converter. In the proposed technique, besides regulating the converter line current and the dc-bus voltages, the switching loss of semiconductor devices was also considered. To do so, four advanced SSs were developed. The proposed technique showed a reduced computational burden than that of the OSS-MPC scheme due to the absence of the weighting factor and having fewer number of SSs. A simulation study was provided to observe the steady-state and dynamic performances of the proposed technique. The power losses under the single- and multiobjective OSS-MPC and the M^{2}PC schemes with the same sampling frequency were compared with that of the proposed ASS-MPC technique. From the simulation study, it was found that the total switching loss of the converter is diminished by almost 50% due to reducing the number of pole SCs per control cycle from four to two when the proposed ASS-MPC scheme is used to control the converter. Moreover, the simulated line current THD of the proposed technique was found to be 2.66%, which is almost similar to that of the single- and multiobjective OSS-MPC schemes. However, the proposed technique showed increased THD of the line current in comparison with the single- and multiobjective M^{2}PC schemes. From the experimental analysis, it was found that the proposed technique shows excellent performance in terms of both the current racking and the dc-bus voltage-balancing ability under various conditions such as sudden change of reference current and supply dc voltage. The experimental harmonic distortion profile of the line current was also included, where the THD was found to be 2.7%. Based on the simulation and the experimental analysis, it was expected that the proposed ASS-MPC technique will help for the widespread application of the NPC MLCs.

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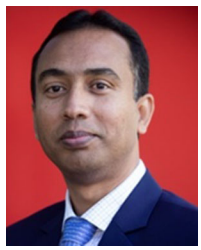

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