ANALYSIS OF HIGH-K AND METAL GATE INFLUENCE ON THE ELECTRICAL BEHAVIOR OF 14 NM DOUBLE-GATE NMOS FETS

A Thesis submitted in partial fulfillment of the requirements for the Award of Degree of Bachelor of Science in Electrical and Electronic Engineering.

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NOVEMBER, 2024

DECLARATION

We hereby declare that this thesis "**Analysis of High-k and Metal Gate Influence on the Electrical Behavior of 14 nm Double-Gate NMOS FETs**" represents our work, which has been done in the laboratories of the Department of Electrical and Electronic Engineering under the Faculty of Engineering of Daffodil International University in partial fulfillment of the requirements for the degree of Bachelor of Science in Electrical and Electronic Engineering and has not been previously included in a thesis or dissertation submitted to this or any other institution for a degree, diploma or other qualifications. We have attempted to identify all the risks related to this research that may arise in conducting this research, obtained the relevant ethical or safety approval (where applicable), and acknowledged my obligations and the rights of the participants.

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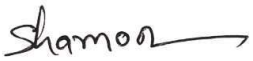

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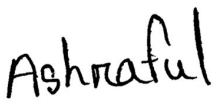

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APPROVAL

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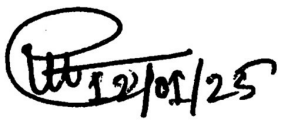

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LIST OF ABBREVIATIONS

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SCEs	Short Channel Effects
DIBL	Drain-Induced Barrier Lowering
SS	Subthreshold Swing
EOT	Effective Oxide Thickness
ASCII	American Standard Code for Information Interchange
ATLAS	Advanced Technology Large Area Silicon
TCAD	Technology Computer-Aided Design
HPC	High-Performance Computer
MATLAB	Matrix Laboratory
CPU	Central Processing Unit
RAM	Random Access Memory
SSD	Solid State Drive
R&D	Research and Development
SDGs	Sustainable Development Goals
AI	Artificial Intelligence
IoT	Internet Of Things
VOCs	Volatile Organic Compounds
BCCSAP	Bangladesh Climate Change Strategy and Action Plan
APRIN	Asia-Pacific Research Integrity Network
EPR	Extended Producer Responsibility
IP	Intellectual Property

IRDS	The International Roadmap for Devices and Systems
ITRS	International Technology Roadmap for Semiconductors
ASIC	Application-Specific Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
SEMI	Semiconductor Equipment and Materials International
AMS	Analog Mixed-Signal
BCCSAP	Bangladesh's Climate Change Strategy and Action Plan
RoHS	Restriction of Hazardous Substances
WEEE	Waste Electrical and Electronic Equipment
DOE	Design of Experiments
ML	Machine Learning
TDDB	Time Dependent Dielectric Breakdown
BTI	Bias Temperature Instability

LIST OF SYMBOLS

Symbol	Name of the symbols
V_{th}	Threshold voltage
V_{fb}	Flat-band voltage
ϕ_f	Fermi potential
Q_f	Fixed charge
C_{ox}	Oxide capacitance per unit area
$\partial t/\partial n$	Rate of change of electron concentration
q	Elementary charge
J_n	Electron current density
G_n	Generation rate of electrons
R_n	Recombination rate of electrons
ϕ_{gate}	Work function of the gate
$\phi_{semiconductor}$	Work function of the semiconductor
Q_{ox}	Oxide charge density
ϵ_{ox}	Permittivity of the oxide material
k	Boltzmann constant
T	Absolute temperature
N_A	Acceptor doping concentration
n_i	Intrinsic carrier concentration
ln	Natural logarithm
Q_b	Bulk charge density (per unit area)
ϵ_{si}	Permittivity of silicon

V_{sb}	Source-to-bulk voltage
t_{ox}	Oxide thickness
I_d	Drain current
μ_n	Electron mobility
W	Channel width
L	Channel length
V_g	Gate voltage
V_d	Drain voltage
λ	Channel-length modulation parameter
n	Electron concentration
E	Electric field
D_n	Electron diffusion coefficient
∇_n	Gradient of the electron concentration
J_p	Hole current density
μ_p	Hole mobility
p	Hole concentration
D_p	Hole diffusion coefficient
∇_p	Gradient of the hole concentration

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ABSTRACT

With the continuous downscaling of metal oxide semiconductor field effect transistors **(MOSFETs)**, the performance and scaling limitations have driven emerging innovative device architectures. In this work, we perform a comprehensive simulation-based study of NMOS design and analysis at **14 nm** with the test-based simulator, **Silvaco TCAD**. Our device has a novel "**sandwich dielectric**" design intended for optimal **threshold voltage (V_{th})** and **I-V characteristics (I_d-V_d)**.

It is suggested that better electrostatic control can be achieved by using a "sandwich" structure made up of a 0.1 nm **zirconium dioxide (ZrO_2)** interface layer, a 0.1 nm **hafnium dioxide (HfO_2)** dielectric layer and a 0.1 nm **silicon nitride (Si_3N_4)** barrier layer. The gate electrode is **tantalum nitride (TaN)** with a work function of 4.3 eV, and the source and drain electrodes are **aluminum (Al)** with a work function of 4.1 eV. Combining these materials with the defined structural arrangement gives better gate control, fewer short-channel effects, and better charge carrier mobility.

Finally, our simulation results suggest that our device has considerably **enhanced electrical performance**. In the form of drain current versus drain voltage (I_d-V_d) characteristics, better control of voltage (V_{th}) and drive currents (I_d-V_d) give higher drive currents, lower leakage current, and better switching performance. To address these challenges, we propose a **double-gate 14 nm NMOS**, a promising device for next-generation **low-power**, **high-power** electronic devices.

This work contributes critically to the field of **nanoelectronics** with a detailed study of material selection, structural innovation, and its impact on device performance. Future research on **advanced MOSFET** architectures and transistor technologies beyond 14 nm can benefit from this study's insights.

CHAPTER 1
INTRODUCTION

1.1 Background of the Study

This advancement is largely fueled by the miniaturization of semiconductor devices over the decades, leading to significant increases in performance and efficiency and a reduction in the size of well-known electronic components. When the transistor dimensions are at the nanoscale, thinning, short-channel effects emerge, leakage currents, threshold voltage instability, etc. Double-gate MOSFETs have been proposed as a potential technology with improved electrostatic control and device performance compared to conventional architectures. In our work, we propose a 14nm double-gate NMOS structure. We also optimize $V_{th,}$ I_d-V_d, $I_{on,}$ and I_{off} properties by using new materials: a barrier layer of silicon nitride (Si_3N_4), an interface material of zirconium dioxide (ZrO_2), and a top high-k dielectric of hafnium dioxide (HfO_2) for the device. Furthermore, we utilize TaN as the gate electrode and Al as the source and drain electrodes to achieve a balanced work function. Using Silvaco TCAD to explore the impact of this material stack on device performance, we aim to improve performance, efficiency, and reliability. Our work enables advances toward scalable transistor architectures, which are crucial for maintaining the cadence of innovation in the semiconductor industry.

1.2 Problem Statement

There are numerous difficulties with the ongoing trend of downscaling the minimum MOSFET sizes to nanoscale dimensions to maximize device performance and reduce power consumption shown in (Fig. 1.2.1) [1]. Short channel effects, gate leakage, and threshold voltage (V_{th}) instability pose significant challenges to device performance and reliability at technology nodes below 14nm. As single-gate MOSFET designs do not afford electrostatic control on the channel, conventional I_d-$V_{d,}$ and device efficiency are degraded. [2]

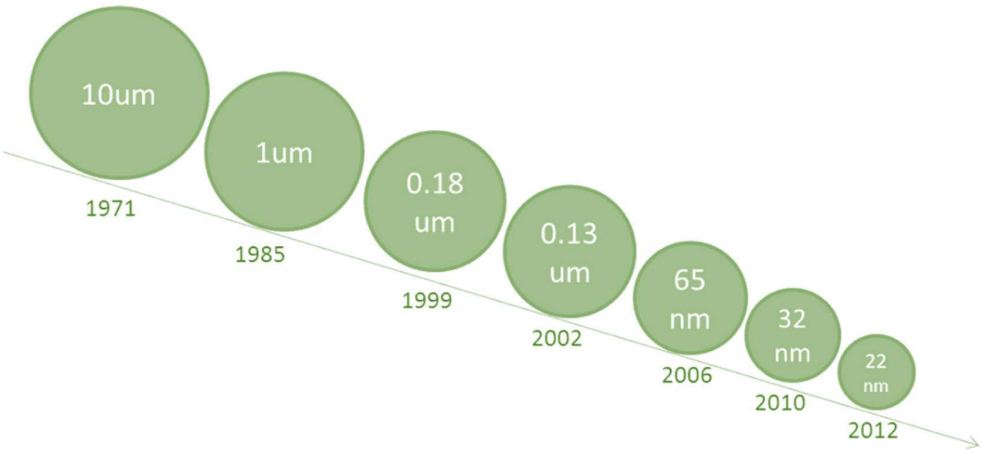

Fig. 1.2.1 Semiconductor Technology Nodes

In particular, double-gate MOSFETs have become viable solutions that provide superior gate control and lower leakage current. However, one must always select optimal materials and layer structures to enhance performance. Device stability and efficiency directly depend on the choice of barrier layers, interface materials, and high-k dielectric. Si_3N_4, HfO_2, and ZrO_2 are being considered in current research for playing these roles [3], but the combined impact on nanoscale double gate designs has been little explored. In addition, achieving a balanced work function in electrode materials, such as TaN and aluminum, is essential in lowering V_{th} and power dissipation. Although there have been advancements made to these materials, there has been little comprehensive study combining these materials within 14nm double-gate NMOS devices using simulation tools such as Silvaco TCAD. Closing these gaps is critical in developing scalable and high-performance semiconductor technologies.

1.3 Objectives

The shrinking transistors present a challenge that we aim to combat by investigating and optimizing the design of a 14nm double-gate NMOS transistor using cutting-edge simulation techniques. Our work in achieving enhanced performance, reliability, and scalability for next-generation semiconductor devices is the ultimate goal. The specific objectives of our thesis are outlined below:

The design and simulation of a 14nm double-gate NMOS structure based on Silvaco TCAD software are exploited to model and analyze accurately nanoscale transistor behavior. We will evaluate the device's performance by examining how various design parameters affect it. [4]

1.3.1 To Optimize Material Selection for Critical Layers in The Transistor:

A barrier layer of silicon nitride (Si_3N_4) for the control of leakage currents. More specifically, zirconium dioxide (ZrO_2) is an interface material for improved dielectric stability. [3]Hafnium dioxide (HfO_2) is a high-k dielectric that improves gate capacitance and lowers the power dissipation barrier layer to control leakage currents. Zirconium dioxide (ZrO_2) is an interface material for improved dielectric stability. Hafnium dioxide (HfO_2) is a high-k dielectric to enhance gate capacitance and reduce power dissipation. Tantalum nitride (TaN) for the gate and aluminum for the source and drain electrodes are analyzed. However, to find out the impact of these electrodes' materials on V_{th} and I_d-V_d properties. The effect of the stacked materials out of the gate stack on the combined short channel effects mitigation, electrostatic control, and overall device performance will be evaluated. [3]

This work compares the proposed design with conventional double-gate MOSFETs for threshold voltage, leakage current, and overall performance metrics.

The objective achievement of these goals is a contribution of our research to the creation of high-performance, scalable transistor architectures suitable for state-of-the-art semiconductor applications.

1.4 Scope of Our Work

Our thesis takes the scope of design, simulation, and study of a 14 nm double-gate NMOS transistor with innovative material combinations to meet the challenge of nanoscale device scaling. Our work aims to push the limits of device performance, reduce power dissipation, and enhance overall reliability for next-generation semiconductor applications. [2]

1.4.1 Device Architecture and Simulation:

Together in this thesis, we use the Silvaco TCAD simulation framework to model and study a 14nm double gate (DG) NMOS structure. As such, we can use this device to assess electrostatic control and short-channel effects and understand how it behaves under a range of operating conditions. [3]

1.4.2 Material Selection and Integration:

It explores the integration of barriers of silicon nitride (Si_3N_4), an interface of zirconium dioxide (ZrO_2), and a high-k dielectric hafnium dioxide (HfO_2). These materials improve threshold voltage stability, leakage currents, and gate capacitance.

1.4.3 Electrode Analysis:

In this thesis, we investigate the effects of using tantalum nitride (TaN) as the gate electrode and aluminum as the source and drain electrodes on work function alignment, threshold voltage, and current characteristics.

1.4.4 Performance Comparison:

In our thesis, we conduct a comparative analysis of the proposed double gate NMOS design with the conventional MOSFET to demonstrate improvements in leakage current, threshold voltage, and overall efficiency.

By providing a design foundation for the realization of high-performance, scalable transistors for advanced applications, this thesis is a key step to the advancement of semiconductor technology.

1.5 Work Schedule

The following Table 1:1 presents the implementation schedule:

Table 1:1 Implementation Schedule

Phase	Task	Timeline (Weeks)
Phase 1: Literature Review and Problem Definition	Conduct an extensive review of the literature on double-gate MOSFETs and material properties. Identify research gaps and define the scope and objectives of the thesis.	Weeks 1–3
Phase 2: Device Design and Material Selection	Design the initial 14nm double-gate NMOS transistor structure using Silvaco TCAD. Select and configure material properties for Si_3N_4, ZrO_2, and HfO_2. - Define work functions for TaN (gate electrode) and aluminum (source/drain).	Weeks 4–6
Phase 3: Simulation Setup and Parameter Optimization	Set up the simulation environment in TCAD with boundary conditions, electrical contacts, and doping profiles. Perform initial simulations to optimize parameters like layer thickness and doping concentration.	Weeks 7–9
Phase 4: Simulation and Data Collection	Run simulations to analyze key performance metrics such as I-V characteristics (I_d-V_d), threshold voltage (V_{th}), and leakage currents. Perform parametric sweeps to study the effects of material and design variations.	Weeks 10–14
Phase 5: Data Analysis and Comparative Study	Analyze simulation results to evaluate the performance of the proposed design. Compare results with conventional double-gate MOSFET designs to validate improvements.	Weeks 15–18
Phase 6: Documentation and finalization	Compile findings, simulation results, and analyses into the thesis document. Review and finalize the thesis for submission.	Weeks 19–20

This structured table ensures clarity in outlining the progression of the research.

CHAPTER 2
LITERATURE REVIEW

2.1 Introduction

Continuous reduction in the size of MOSFETs to 14 nm technology is enabling device structure, material selection, and fabrication techniques to advance. As devices shrink, issues such as SCEs, leakage currents, and V_{th} instability become more significant. To solve them, the gate structure and dielectric material, as well as the barrier layer, have been researched. This chapter functions as a detailed review of the prior research in these areas, identifying important contributions, limitations, and remaining research directions.

Another major step toward improving MOSFET design has been the evolution from single-layer dielectrics to high-k materials such as HfO_2. However, the leakage current and V_{th} variability issues necessitate further investigations into structures with multi-layer dielectric. The dual-gate architectures have been investigated recently to better electrostatically control device operation and alleviate short-channel effects. As V_{th} has become a more important metric of device reliability, barrier layers such as Si_3N_4 and advanced gate materials such as TaN have gained traction for incorporation into the device structure.

2.2 Review of Related Research

Due to the increasing need for high-performance, low-power, scalable semiconductor technology, there has been extensive research on the design and optimization of 14 nm double-gate NMOS devices. In this section, we review key studies on material engineering, dielectric design, and gate control techniques for advanced NMOS devices. We demonstrate the relevance of our proposed multi-layer dielectric system and discuss the contributions, methodologies, and limitations of previous works.

2.2.1 Short-Channel Effects (SCE) Mitigation

As devices scale into smaller dimensions, short channel effects (SCEs), such as drain-induced barrier lowering (DIBL) and sub-threshold leakage, become more significant.

Regarding multi-gate structures, where FinFETs and double-gate MOSFETs were used to enhance the electrostatic control on the channel. Our work showed that reducing SCEs is orders of magnitude more effective with double gate designs than with planar MOSFETs. However, silicon dioxide (SiO_2) and single-layer dielectrics became ineffective at smaller nodes in their approach. [5]

Then proposed subsequently using high-k dielectrics such as HfO_2 to improve the gate control and reduce leakage. This approach reduced leakage current, but single-layer high-k dielectrics were not able to sufficiently control the channel at the 14nm scale. We use what we've learned to make a tri-layer dielectric (SiN_4, ZrO_2, and HfO_2) that works better than single-layer solutions for improved gate channel coupling and SCE reduction. [6]

2.2.2 Leakage Current Suppression

As gate oxide thickness decreases, leakage current becomes a potential problem. When HfO_2 high-k dielectrics and TaN gate electrodes come into direct contact with each other, the number of interface traps and leakage currents go up. To tackle this problem, they suggested using the technique of interface engineering. Their work identified the role of interface defects, but it did not propose a specific barrier layer to prevent interactions. [7]

Other work investigated the effect of alternative dielectric materials on leakage. For illustration, [8]explored the use of ZrO_2 instead of HfO_2. According to their findings, ZrO_2 has a higher band gap than mullite, which results in better leakage control, but their compatibility with standard CMOS fabrication processes is somewhat limited. We get around this problem by using a "sandwich" structure made up of layers of Si_3N_4 barrier, ZrO_2, and HfO_2. This balances gate capacitance and leakage control.

2.2.3 Threshold Voltage (V_{th}) Stability

NMOS device operation at small nodes requires V_{th} stability, which is therefore critical. One commonly observed cause of variation in V_{th} is the work function of metal gate fluctuations or defects at the gate dielectric interface. According to [7]the V_{th} shift can be quite big if there isn't a good barrier layer between the HfO_2 dielectric and the TaN

gate. This is because the charge can get stuck in the interface. In their research, they explored the necessity of a barrier layer, but they did not propose a specific solution.

Based on this insight, [9]have recently studied the influence of thin barrier layers such as Si_3N_4 on V_{th} stability. By keeping ultra-thin Si_3N_4 barriers, they found that it reduces charge trapping while maintaining compatibility with high-k dielectrics. We kept the V_{th} stable by stopping charge trapping and work function changes in our study by adding a 0.1 nm Si_3N_4 barrier layer between the ZrO_2/HfO_2 stack and the TaN gate.

2.2.4 Dielectric Engineering and Multi-Layer Integration

The shift from single-layer to multi-layer dielectrics has become a key focus in MOSFET design. Research by [6]emphasized the limitations of single-layer HfO_2, which led to increased leakage and reliability issues. Studies have since explored the integration of ZrO_2 and HfO_2 in multilayer configurations. [10]demonstrated that ZrO_2/HfO_2 stacks improved gate capacitance and leakage performance. However, their approach did not incorporate an additional barrier layer to address interface defects.

Our method uses a three-layer dielectric system (Si_3N_4, ZrO_2, and HfO_2). The Si_3N_4 layer blocks electricity flow and the ZrO_2/HfO_2 stack improves capacitance and leakage. This approach provides a more holistic solution, addressing both interface stability and leakage suppression. Silvaco TCAD simulations validate the effectiveness of this approach in terms of V_{th} stability, leakage current reduction, and enhanced drive current (I_d).

2.2.5 Simulation-Based Design and Optimization

Modeling sub-20 nm MOSFETs has relied heavily on the use of simulation tools like Silvaco TCAD. The work of [9]demonstrates its use to understand (these include V_{th}, subthreshold swing, and leakage current) in the case of double gate and FinFET structures. However, their work concentrated on single-layer dielectric materials and did not consider multi-layer approaches.

We extend this work in our study by simulating a 14nm double-gate NMOS with a multi-layer dielectric (Si_3N_4, ZrO_2, HfO_2) and a TaN gate using Silvaco TCAD. We perform detailed simulation analysis of V_{th}, I_d-V_d, leakage, and short channel effects.

This approach provides a complete evaluation of the device's performance, surpassing the current simulation-based research.

2.3 Comparison and Analysis of Previous Work

Double-gate NMOS technology for 14nm has advanced significantly in designs of gate structures, dielectrics, and interface engineering shown in (Fig. 2.3.1).

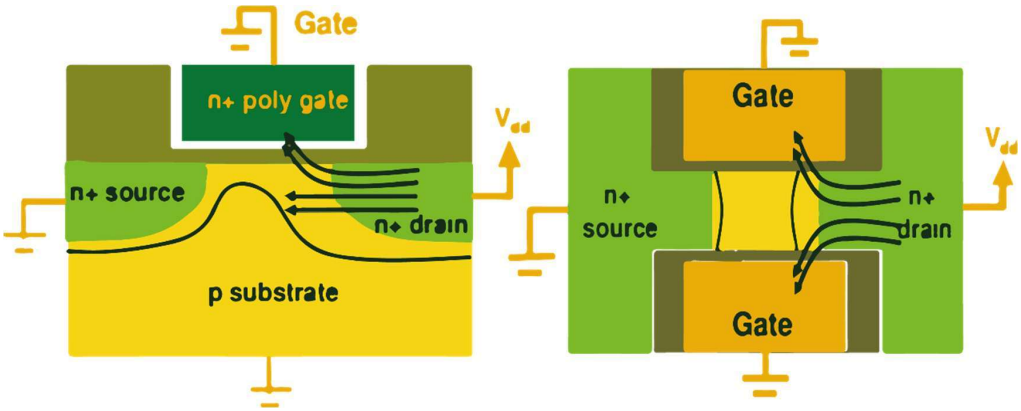

Fig. 2.3.1 Single Gate to Double Gate MOSFET

While previous studies have made significant contributions to steadying V_{th} and suppressing leakage, several limitations remain unresolved. Here, we provide a comparative analysis of previous research before explaining how our investigation fills these gaps.

2.3.1 Gate Structure and Control

Previous work: [5]pioneered the use of double-gate structures to enhance electrostatic control and proposed a preference for dual-gate structures over planar MOSFETs. [6]extended this approach with high-k gate dielectrics to improve gate channel coupling and subthreshold leakage. Yet, these works have solely relied on single-layer dielectrics (e.g., HfO_2) and no barrier to address V_{th} variability and interface defects.

Our Approach: In contrast to earlier designs, our 14nm double-gate NMOS utilizes a tri-layer dielectric (Si_3N_4, ZrO_2, HfO_2) and a TaN gate. It lowers interface defects with

the Si_3N_4 barrier layer, and adding ZrO_2 and HfO_2 makes gate-channel control and capacitance better. Based on Silvaco TCAD simulations, it also improves channel electrostatics control and mitigates short-channel effects (SCEs).

2.3.2 Dielectric Material Selection

Previous Work: Previous works largely used single-layer high-k dielectrics, like HfO_2 [6], or other materials, like ZrO_2 [8]. To address leakage and improve the capacitance, [10]introduced a ZrO_2/HfO_2 dual-layer system. These approaches increased device performance, but single- and dual-layer dielectrics did not provide adequate protection against interface charge trapping and V_{th} variability shown in (Fig. 2.3.2) [11].

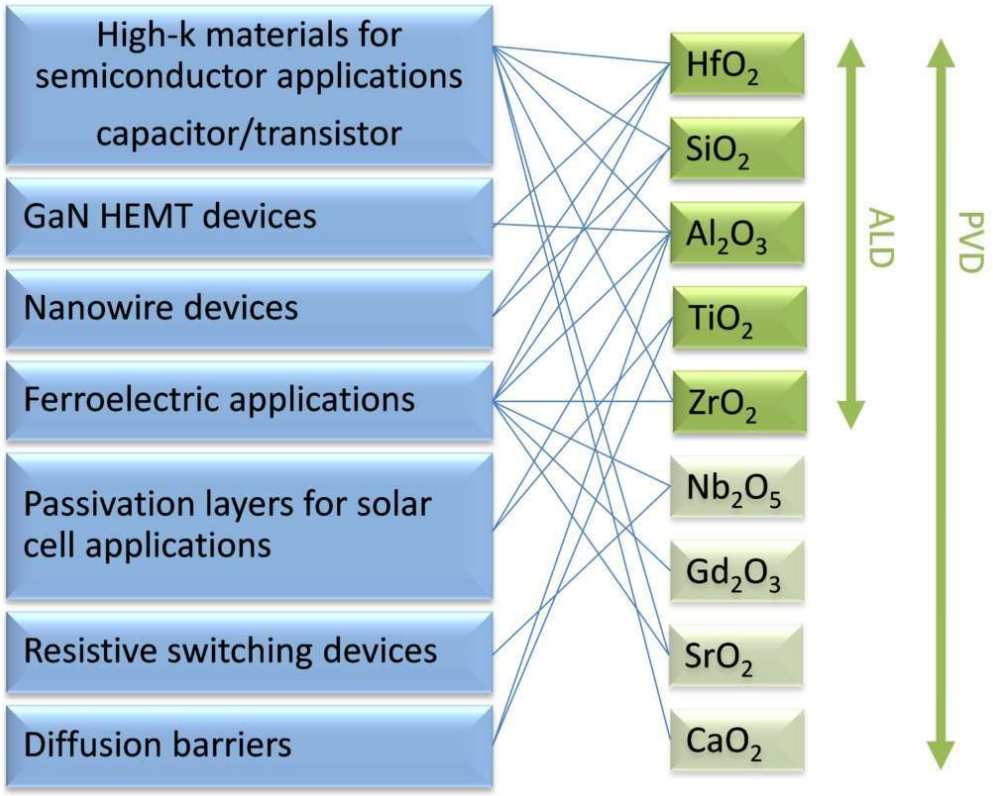

Fig. 2.3.2 Various Kinds of Dielectric Materials

Our Approach: We extend the concept of multi-layer dielectrics to a tri-layer 'sandwich' configuration consisting of Si_3N_4, ZrO_2, and HfO_2. An interface protection

layer is formed by the Si_3N_4 barrier layer, which prevents charge trapping at the TaN gate interface. Leakage current is suppressed better by the ZrO_2 layer and improved gate capacitance is provided by the HfO_2 layer. With this dual-layer combination, we achieve better leakage control, higher gate capacitance, and better V_{th} stability than previously reached through dual-layer approaches.

2.3.3 Leakage Current Suppression

Previous Work: Penetration of electrons into the HfO_2 dielectric layer by direct contact of the TaN gate with it through interfacial defects and charge trapping was reported by [7] to cause leakage current increase. The current study highlights the importance of interface engineering without proposing a specific solution to this issue. However, [8]demonstrated that ZrO_2 has superior leakage suppression compared to HfO_2 due to its higher band gap, but they did not propose a practical implementation of the multi-layer structure.

Our Approach: To address this, we integrate an ultra-thin (0.1 nm) Si_3N_4 barrier layer between the TaN gate and the ZrO_2/HfO_2 stack. This barrier reduces interface charge trapping and prevents direct interaction between TaN and high dielectrics. We exploit the superposition of ZrO_2 and HfO_2 layers in a novel sandwich-like configuration to realize leakage suppression beyond that of single and dual layers. Our design significantly reduces leakage current according to Silvaco TCAD simulations.

2.3.4 Threshold Voltage (V_{th}) Stability

Previous Work: According to [7]work function variability and charge trapping at the gate-dielectric interface are the main sources of V_{th} fluctuations. Their work showed the need for barrier layers but did not suggest a practical solution for sub-20nm devices. [9] investigated the defects at the interface on V_{th} variability and how we can use thin barrier layers such as Si_3N_4. While their study confirmed that ultra-thin barriers could be used to stabilize V_{th}, their simulation was not run for a tri-layer dielectric system.

Our Approach: To minimize both charge trapping and work function variability, we include an ultra-thin (0.1 nm) Si_3N_4 barrier between the TaN gate and a stack of dielectrics. Better V_{th} stability than previous approaches is provided by this design.

Finally, V_{th} control is further strengthened by our tri-layer system (Si_3N_4, ZrO_2, HfO_2), as verified by our Silvaco TCAD simulations. We find that our approach minimizes V_{th} fluctuations better than approaches that only use single-layer or dual-layer dielectrics.

2.3.5 Simulation and Design Validation

Previous Work: The device performance was modeled via double-gate MOSFETs based on Silvaco TCAD and then assessed by [9]. [9]focused their simulations on V_{th}, subthreshold swing, and leakage current. However, they limited their work to single-layer dielectric models, avoiding multi-layer configurations.

Our Approach: Following these simulation-based studies, we use Silvaco TCAD to model and analyze a tri-layer dielectric structure (Si_3N_4, ZrO_2, HfO_2) in a 14nm double-gate NMOS. We comprehensively evaluate the performance of our device through analysis of V_{th}, I_d-V_d characteristics, leakage current, and short-channel effects. Validated with our multi-layer design, our results show improvements in leakage current, short channel control, and V_{th} stability.

2.4 Gaps Addressed by Our Investigation

Short channel effects (SCEs), leakage currents, unstable threshold voltage (V_{th}), and changes in device performance are some of the performance and reliability issues that come up as MOSFETs get smaller and smaller, all the way down to sub-20 nm. While the previous work on these issues has made significant strides, there are still key gaps in material integration, dielectric multilayer design, and work function engineering. Our contribution to these gaps is based on a novel integration of TaN, Si_3N_4, ZrO_2, and HfO_2 into a 14nm double-gate NMOS structure. We briefly describe the gaps our research fills in the following areas.

2.4.1 Enhanced Control of Short-Channel Effects (SCEs)

[5]identified the gap, demonstrating that double-gate MOSFETs reduce short-channel effects compared to single-gate devices. Although it was reliant on silicon-based materials, the device could not completely suppress SCEs at the ultra-scaled dimensions. However, it did not explore the use of advanced multi-layer dielectrics or interface engineering.

Our contribution: In this thesis, we fill in this gap by adding a multi-layer dielectric stack (Si_3N_4, ZrO_2, HfO_2) that controls gate channel electrostatics better. Such a configuration mitigates drain-induced barrier lowering (DIBL) and subthreshold swing (SS), two key short-channel effects that degrade device performance. We show that our structure gives improved channel control over single-layer dielectric designs using Silvaco TCAD simulations.

2.4.2 Improved Leakage Current Suppression

Identified Gap: For instance, [6]studied the use of HfO_2 as a high-k dielectric to lower leakage current without exploring the subsequent possibility of multilayer dielectric stacks. In the single-layer HfO_2 system, leakage current control was not possible at ultra-thin dielectric thicknesses.

Our Contribution: We fill this gap by looking at a multi-layer dielectric of 0.1 nm HfO_2, 0.1 nm ZrO_2, and 0.1 nm Si_3N_4. The high-k properties of HfO_2, ZrO_2, and Si_3N_4 barrier layer further reduce leakage current suppression due to the high interface state density of HfO_2 compared to ZrO_2 while offering additional resistance to tunneling currents. One of the important advantages of this approach over devices with a single-layer HfO_2 gate dielectric is that the total leakage current is decreased. TCAD simulations with Silvaco confirm that the multi-layer stack significantly reduces off-state leakage currents, thereby boosting power efficiency.

2.4.3 Threshold Voltage (V_{th}) Stability and Variability

Identified Gap: [7]reported that gate electrode material selection has a significant impact on V_{th} stability. First, they showed that TaN (work function ~ 4.4 eV) is suitable for NMOS devices, but they did not examine how the addition of barrier layers would affect V_{th}. However, in the absence of barrier layers like Si_3N_4, the gate was more sensitive to work function fluctuations due to interface state and process variations.

Our Contribution: To fill this gap, we introduce a 0.1 nm thick Si_3N_4 barrier layer between a TaN gate electrode (work function ~ 4.3 eV) and a multi-layer dielectric stack (ZrO_2 and HfO_2). Stabilization of the interface reduces V_{th} variability due to the Si_3N_4 layer that mitigates work function fluctuations. This innovation permits V_{th} to

remain stable in the presence of process-induced variability. When we simulate our devices, we show that their V_{th} values are statistically more stable than those of devices with a direct TaN-HfO_2 interface. We also see that the threshold voltage drifts more steadily over time.

2.5 Multi-Layer Dielectric Stack for Enhanced Capacitance

Identified Gap: [6]have studied the use of single-layer HfO_2 as the gate dielectric but have not investigated multi-layer stack configurations. When it comes to apparatus scalability, leakage control, and effective oxide thickness (EOT), single-layer structures have limitations.

Our Contribution: We introduce a trio-layer dielectric stack of Si_3N_4, ZrO_2, and HfO_2. In turn, this design provides lower effective oxide thickness (EOT) with leakage current suppression. By using high-k materials (ZrO_2 and HfO_2) with the stable barrier property of Si_3N_4, better interface stability and improved electrostatic control can be achieved. Reduced EOT enhances the gate-channel capacitance, which in turn boosts the I_d of the device. As confirmed by our Silvaco TCAD simulations, this leads to higher gate capacitance and lower leakage currents than single-layer HfO_2 designs.

2.5.1 Comprehensive Simulation of Advanced Material Combinations

Identified Gap: However, [9]simulated and studied sub-20nm double-gate MOSFETs for conventional silicon-based materials. However, their work did not account for how the performance would be impacted when stacks and barrier layers are multiple materials.

Our Contribution: To fill this gap, we perform extensive Silvaco TCAD simulation of a complete multilayer material system comprising a TaN gate, a Si_3N_4 barrier, and multiple-layer dielectrics (ZrO_2 and HfO_2). Through our simulation methodology, we can evaluate key performance measures including threshold voltage (V_{th}), I_d-V_d, leakage current, and short channel effects. Utilizing multi-material analysis, we complete a comprehensive analysis of device performance beyond the scope of [9] as shown in Table 2:1.

Table 2:1 Summary of addressed Gaps

Gap	Previous Research	Our Contribution
Short-channel effects	Chau et al. (2004) - Si-based MOSFETs [12]	Multi-layer dielectric stack for better control
Leakage current	Park et al. (2010) - HfO_2-only designs [13]	Multi-layer dielectric (Si_3N_4, ZrO_2, HfO_2) stack
Threshold voltage (V_{th})	Yang et al. (2013) - No barrier layer [7]	Si_3N_4 barrier layer for enhanced V_{th} stability
Dielectric stack design	Park et al. (2010) - Single-layer HfO_2 [6]	Multi-layer stack for improved capacitance
Advanced simulations	Silva et al. (2018) - Conventional stack [9]	Multi-material analysis of the entire device

2.6 Summary

In Chapter 2, an elaborate review of existing work on 14 nm double-gate NMOS device design and optimization were presented. Key focus areas included material selection, dielectric engineering, and design of gate electrodes to mitigate short channel effects (SCE), control leakage currents and stabilize threshold voltage (V_{th}).

Previous studies showed the single-layer high-k dielectrics as HfO_2, but these designs had trouble controlling leaks and maintaining V_{th} stability. [5]stressed the point of multi-gate structures to reduce SCEs, and [6] searched for high-k materials to refine the gate control. However, the inadequacy of single-layer dielectrics necessitated the need for more sophisticated material integration.

We show that both a multi-layer dielectric stack and the addition of a barrier layer are necessary to improve device performance. Our approach helped to fill these gaps in previous works, including limited leakage suppression, instability in $V_{th,}$ and lack of thorough analysis of material interfaces. Our design attempts to incorporate a TaN gate, a Si_3N_4 barrier, and a tri-layer dielectric (Si_3N_4, ZrO_2, HfO_2) to provide the best possible short channel control, reduced leakage current and improved V_{th} stability.

In this chapter, we also reviewed simulation methods and as a special focus, the capabilities of Silvaco TCAD for multi-material and multilayer device

modeling. Previous studies, for example, [9], have shown the applicability of simulation-based optimization to the design of advanced MOSFETs but only partially explored the integration of multiple materials in a sandwich dielectric configuration.

Overall, the literature review has established the relevance and significance of our approach to the challenge of the enormous demand for a complete multi-layer dielectric system. Using this design, we close the gaps that we identified, improving the performance, scalability, and reliability of future-generation nanoscale NMOS devices.

CHAPTER 3
METHODOLOGY

3.1 Introduction

We then describe in this chapter how we designed, simulated, and analyzed the double-gate 14 nm NMOS transistor in Fig. 3.1.1 using a detailed and systematic approach. In our methodology, careful material selection (see Fig. 3.1.2 and Fig. 3.1.3), precise device design, simulation setup with Silvaco TCAD, and iterative optimization of critical parameters are stressed to attain significant V_{th} and I_d-V_d current characteristics. [12] The process was planned, executed, and reviewed extremely carefully to match it to the research object and to gather meaningful contributions to the field of advanced transistor technologies. [13] [14]

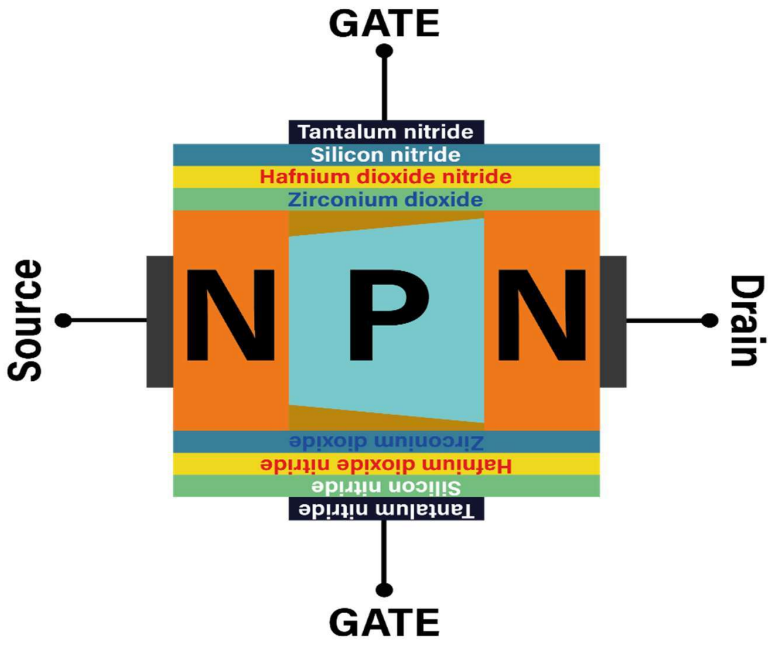

Fig. 3.1.1 “14 nm Double-Gate NMOS FETs”

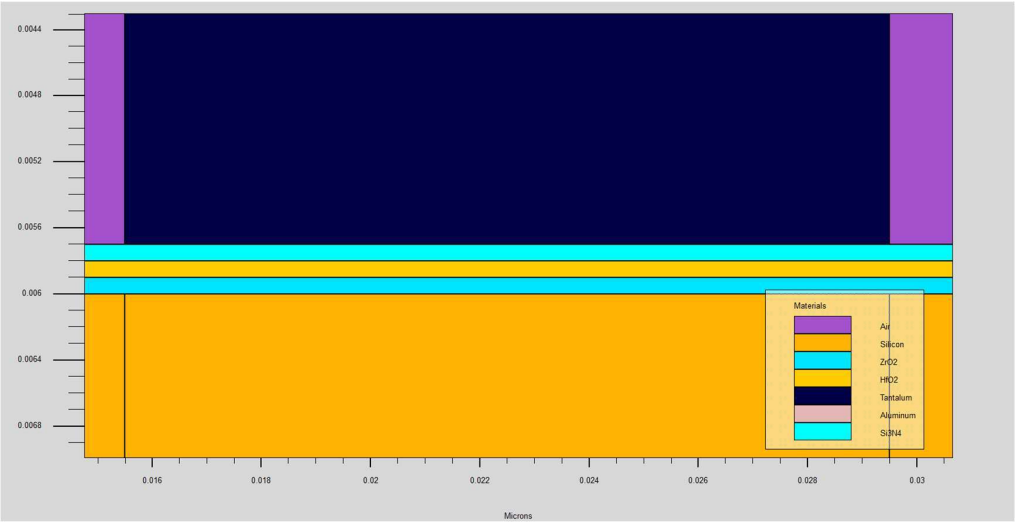

Fig. 3.1.2 Material Stack Under Gate-1

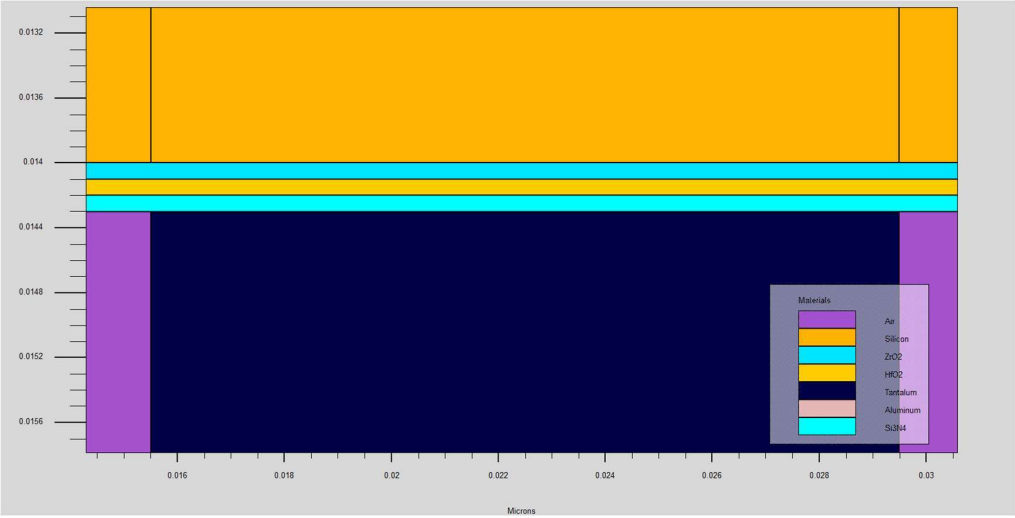

Fig. 3.1.3 Material Stack Under Gate-2

3.2 Material Selection and Properties

So, we carefully chose our materials to optimize device performance and make them compatible. We discuss the chosen materials and their respective roles in the transistor design below:

3.2.1 Barrier Layer:

For its excellent insulating properties and very low leakage current reduction effectiveness, we chose silicon nitride (Si_3N_4) (Fig. 3.2.1) of 0.1 nm thickness (Fig. 3.2.2). [15] Because of its high thermal stability and compatibility with high-k dielectrics, it is an ideal choice for use as a barrier layer in the advanced transistor. [13]

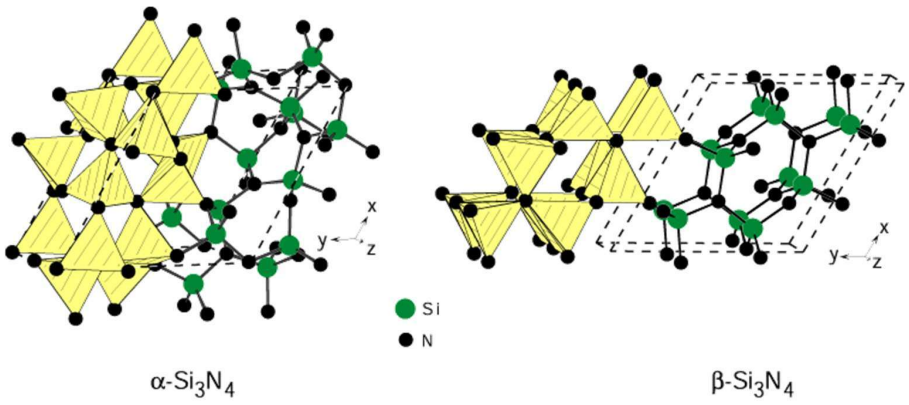

Fig. 3.2.1 Structural Isomers of Silicon Nitride (Si_3N_4)

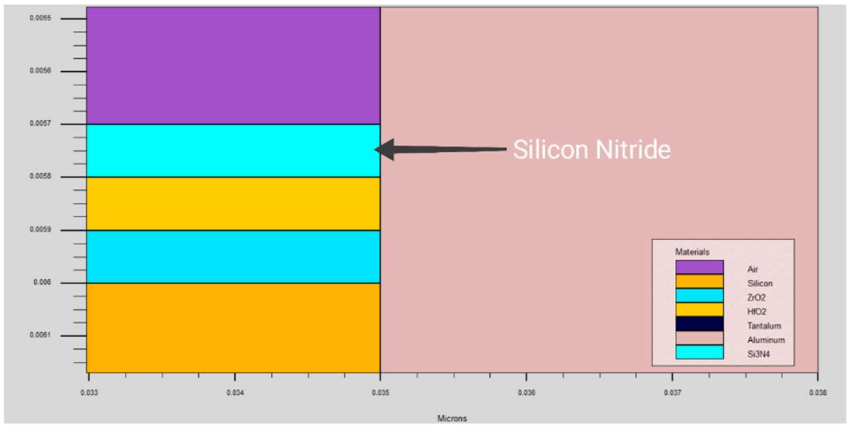

Fig. 3.2.2 Silicon Nitride Implantation

3.2.2 Interface Layer:

Our interface layer is zirconium dioxide (ZrO_2) (Fig. 3.2.3) with a thickness of 0.1 nm (Fig. 3.2.4) [16] and is chosen for its high dielectric constant that, as a result, increases the gate capacitance and improves the channel stability. Under nanoscale operation, reliable device performance is ensured through its strong thermodynamic compatibility with HfO_2 and Si_3N_4. [17]

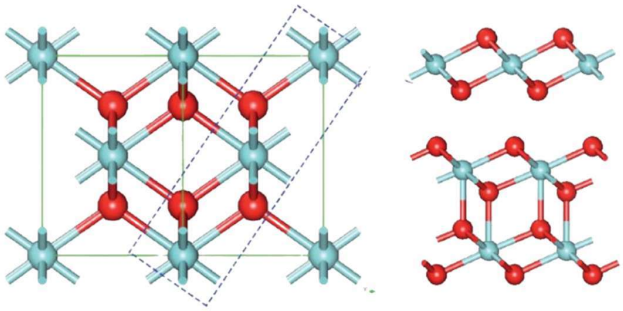

Fig. 3.2.3 Structural Isomers of Zirconium Dioxide (ZrO_2)

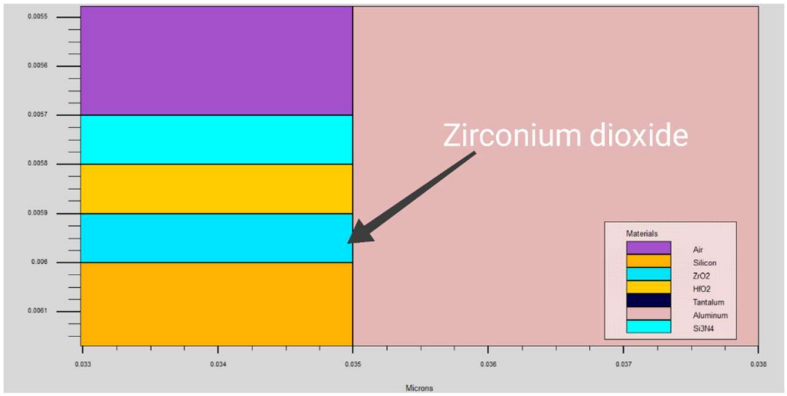

Fig. 3.2.4 Zirconium Dioxide Implantation

3.2.3 Dielectric Layer:

We incorporated hafnium dioxide (HfO_2) (Fig. 3.2.5) as the primary gate dielectric layer, with a thickness of 0.1 nm (Fig. 3.2.6) [18]. Its high permittivity (k-value) and

reduced leakage current properties improve gate control while maintaining scalability. The material is well-suited for high-performance transistor designs. [19]

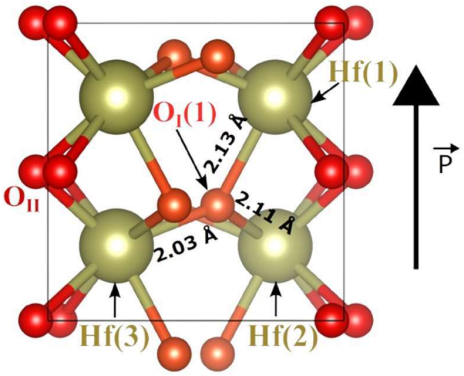

Fig. 3.2.5 Structural Isomers of Hafnium Dioxide (HfO_2)

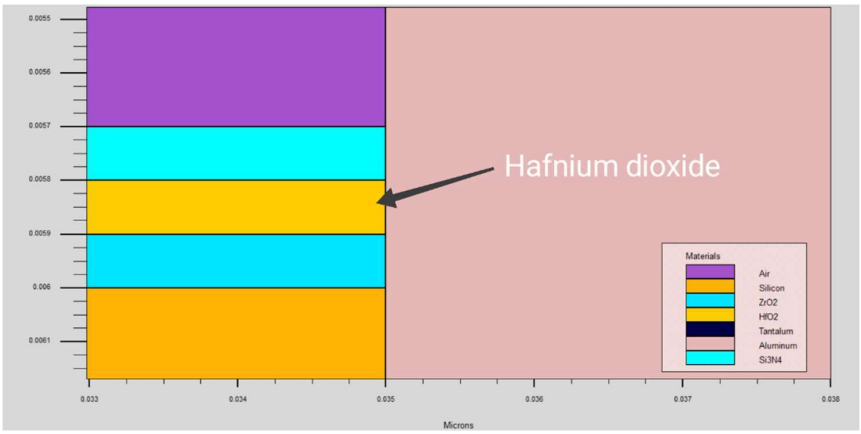

Fig. 3.2.6 Hafnium Dioxide Implantation

3.2.4 Gate Electrode:

We chose tantalum nitride (TaN) (Fig. 3.2.7) with a work function of 4.3 eV as the gate electrode material (Fig. 3.2.8) [20]. Due to their excellent stability, compatibility with high-K dielectrics, and ability to provide accurate sub-nanometer channel control, TaN is extremely well suited for nanoscale devices. [21]

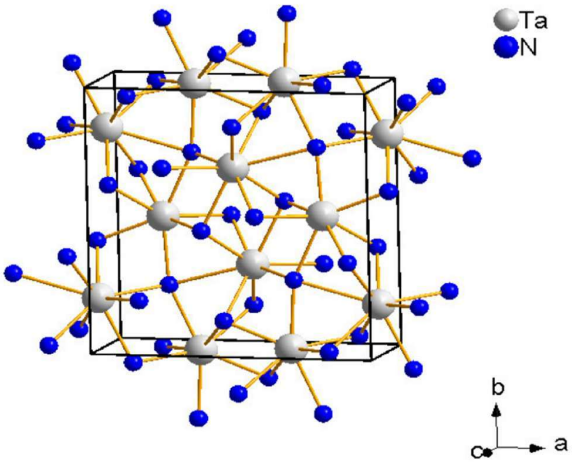

Fig. 3.2.7 Structural Isomers of Tantalum Nitride (TaN)

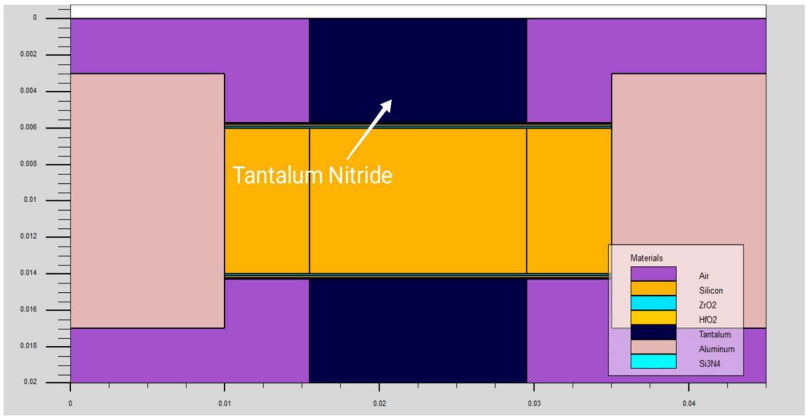

Fig. 3.2.8 Tantalum Nitride Implantation

3.2.5 Source and Drain Electrodes:

We selected aluminum (Fig. 3.2.9) as the source and drain electrode material due to its 4.1 eV work function. Low contact resistance in combination with high conductivity offers excellent current injection, thus supporting higher I_d-V_d performance and overall device efficiency. [22]

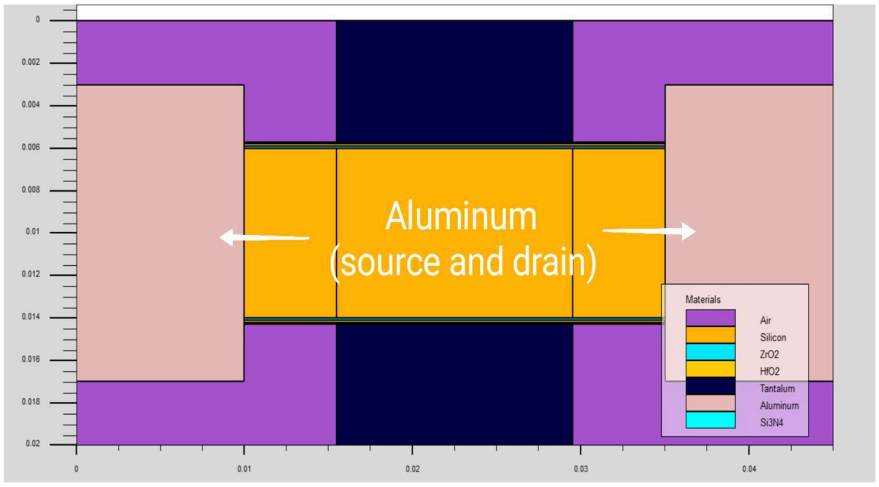

Fig. 3.2.9 Aluminum Implantation

3.3 Design Specifications and Constraints

The design of our double-gate NMOS transistor followed specific guidelines to achieve nanoscale efficiency. We outline the key specifications and constraints below:

3.3.1 Gate Length:

We set the transistor's gate length to 14 nm to align with industry standards for advanced scaling (Fig. 3.3.1). This length guarantees electrical robustness while maintaining static compatibility with high-density integration. However, a shorter gate length improves device speed but needs tight control to tolerate leakage and short channel effects.

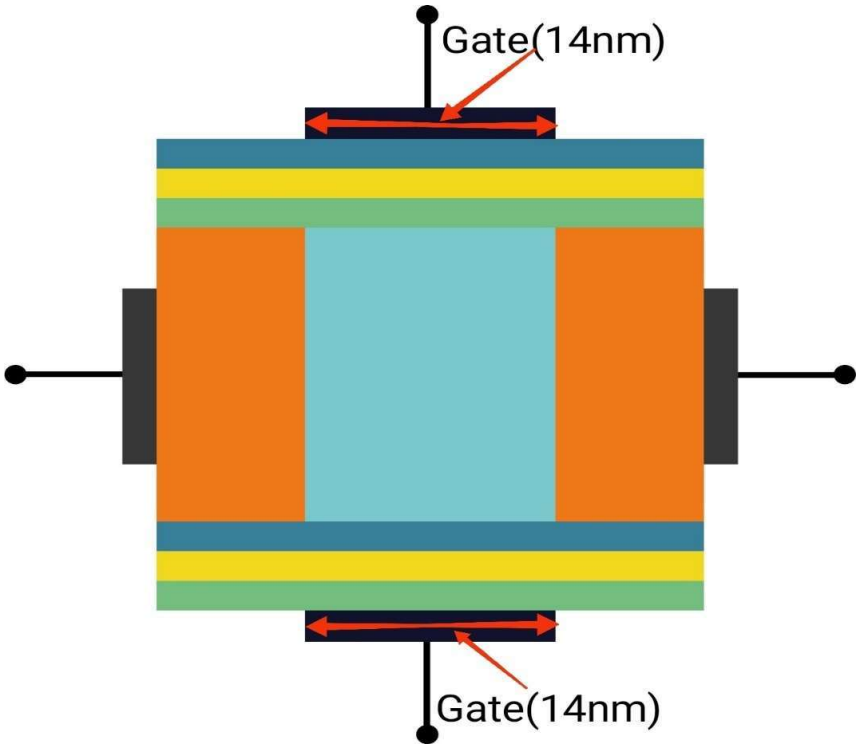

Fig. 3.3.1 Gate Length

3.3.2 Channel Structure:

Channel control is improved and the short channel effect is reduced in a double gate architecture. This design improves the electrostatic control over the channel (Fig. 3.3.2), which leads to better modulation of the carrier flow, as well as decreasing parasitic effects. Indeed, a double-gate structure is very effective for nanoscale devices where single-gate design is plagued by leakage and control issues.

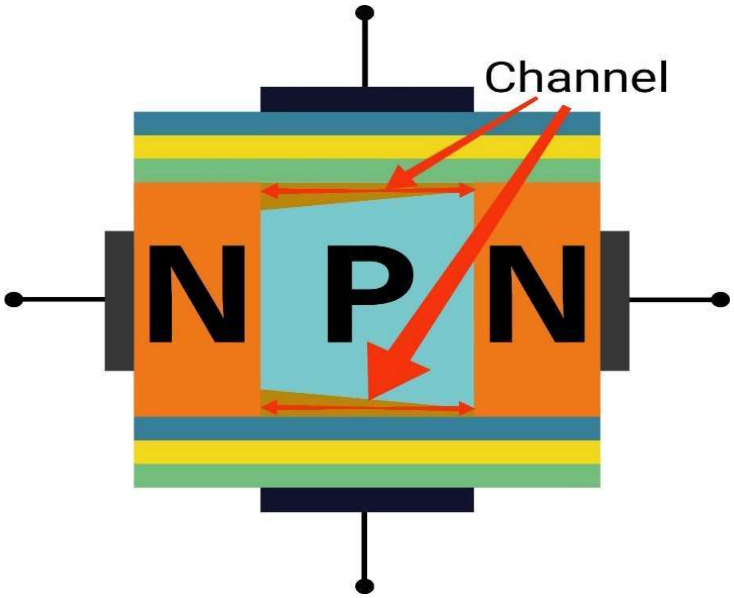

Fig. 3.3.2 Channel Structure

3.3.3 Simulation Parameters:

We use layer thicknesses and doping concentrations to accurately represent real conditions.

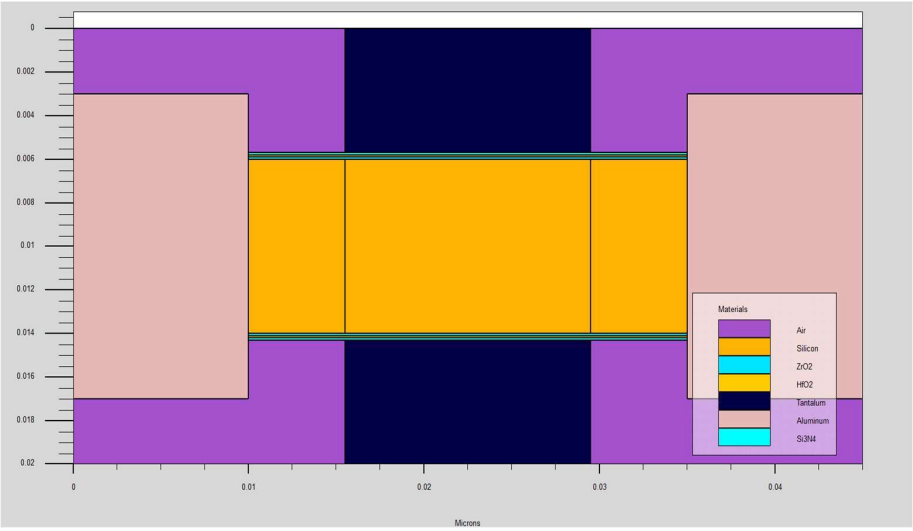

Fig. 3.3.3 Simulation Structure

We made sure that the barrier layer (Si_3N_4), interface layer (ZrO_2), and dielectric (HfO_2) were all 0.1 nm thick so that there was a balance between lowering leakage and increasing capacitance, as shown in Fig. 3.3.3.

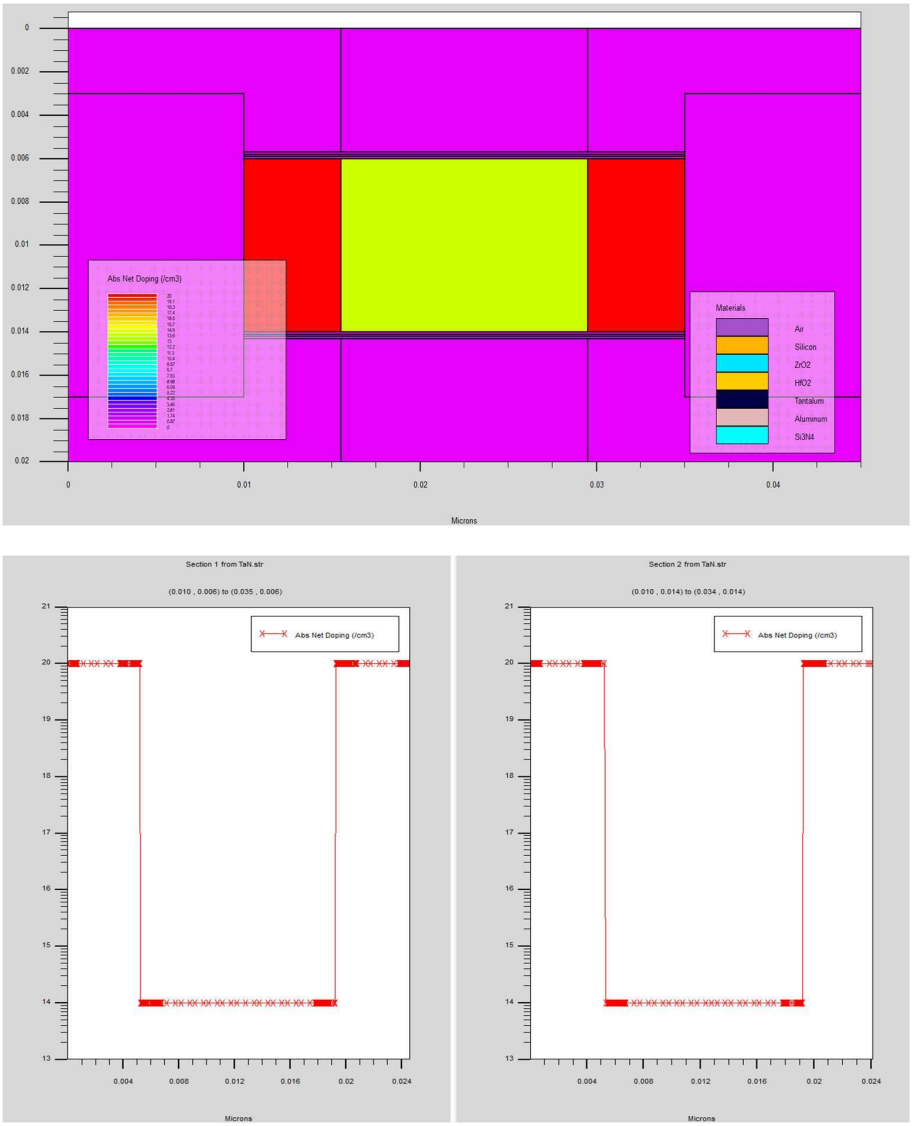

Fig. 3.3.4 Doping Concertation Profile

Doping concentrations of 1×10^{20} cm^{-3} for the source and drain and 1×10^{14} cm^{-3} for the channel ensure effective carrier modulation shown in Fig. 3.3.4.

3.4 Simulation Setup with Silvaco TCAD

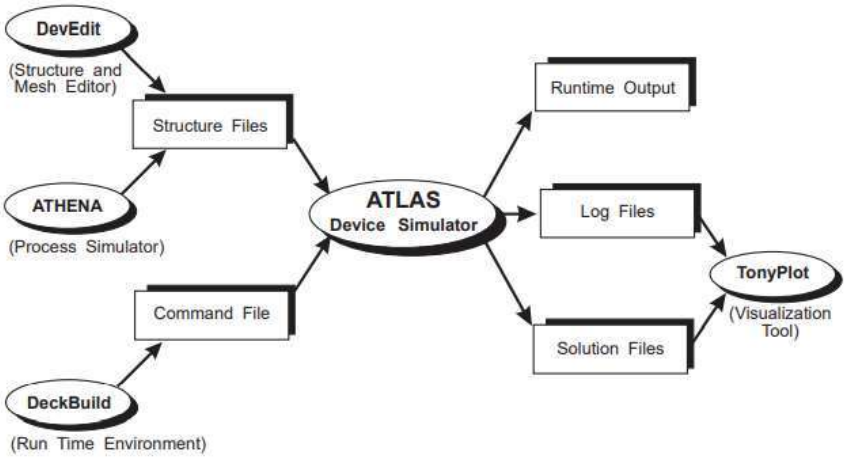

Fig. 3.4.1 Silvaco TCAD Flowchart

The simulation setup in Silvaco TCAD Atlas is defined by 14nm double gate NMOS with Si_3N_4 barrier, ZrO_2 interface, HfO_2 dielectric, TaN gate, and aluminum electrodes for the analysis of V_{th}, I_d-V_d Shown in Fig. 3.4.1 [23] and Fig. 3.4.2.

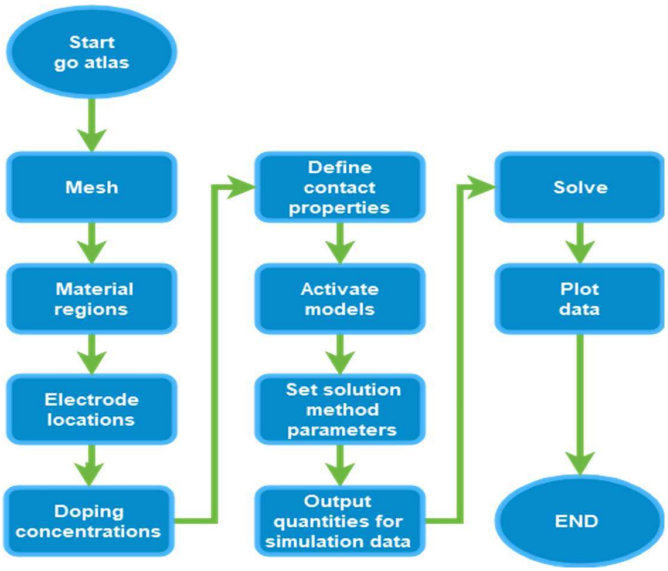

Fig. 3.4.2 Our simulation flowchart

3.4.1 Device Construction

The Silvaco TCAD platform used the ALTAS module to construct both the physical structure (the 14 nm double gate NMOS transistor) and the device layer of the 14 nm short channel NMOS transistor. This module allowed us to precisely stack materials, define layer thicknesses, and introduce doping profiles. Using the toolkit's ALTAS, a simple ASCII and binary layer file format, we modeled the device layer by layer, from the silicon substrate to the aluminum source and drain electrodes. High-accuracy deposition of each material layer as Si_3N_4, ZrO_2, HfO_2, and TaN was achieved to faithfully reproduce the double-gate structure. Together with advanced etching, it also refined the architecture and matched real-world manufacturing scenarios and our Device Construction Summary shown in (Table 3:1).

Table 3:1 Device Construction Summary

Layer/Step	Material	Thickness (nm)	Purpose
Substrate	Silicon	5.6nm	Base layer for device construction.
Barrier Layer	Si_3N_4	0.1nm	Reduces leakage current.
Interface Layer	ZrO_2	0.1nm	Provides high interface stability.
Dielectric Layer	HfO_2	0.1nm	Acts as the primary gate dielectric.
Gate Electrode	TaN	3.4nm	Enables gate control with 4.3 eV work function.
Source/Drain	Aluminum	9.8nm	Facilitates current flow with low contact resistance.

3.4.2 Electrical Simulation

The electrical performance of the NMOS device was simulated using the ATLAS module, emphasizing important parameters such as V_{th} and I_d-V_d under various operating conditions. ATLAS accurately models the transport physics, interface interactions, and carrier dynamics through different layers. This kind of electrical analysis makes it easier to look into how the interface and dielectric layers affect the

overall efficiency, scalability, and performance metrics of the device when biasing situations, temperature changes, and material interactions happen.

3.4.3 Parameter Tuning

We used ATLAS modules to iteratively optimize the design parameters, such as material thicknesses, doping concentrations, and interface properties. We aimed to enhance the device by tuning the highest V_{th}, highest I_d-$V_{d,}$ and overall device stability. Electric characteristics were refined through iterative adjustments made to Si_3N_4, ZrO_2, HfO_2, and dopant profiles, keeping scalability in mind. Through such fine-tuning, short channel effects were minimized and the device adhered to industry performance standards in advanced 14 nm technologies.

3.5 Analytical Approach

We systematically compared our results to data from similar devices in the literature to validate the simulation outcomes. Within this comparative analysis, we sought to compare critical performance metrics to ensure that our design modifications conformed to industry benchmarks and maximized device efficiency.

3.5.1 Threshold Voltage (V_{th})

To determine the threshold voltage, we used the linear extrapolation technique, a common method for extracting the transistor's state value. In this method, first, I_d vs V_g was plotted and the intersection of the extrapolated linear region was found by finding the intersection of the V_g axis. This parameter is critical to assessing switching behavior, making turn-on characteristics, and achieving low leakage currents.

The threshold voltage can be expressed as:

$$V_{th} = V_{fb} + 2\phi_f + \frac{Q_f}{C_{ox}}$$

Where:

V_{fb}: Work function difference between gate material and semiconductor and any fixed charges at the oxide-semiconductor interface accounted for in the flat band voltage.

$$V_{fb} = \phi_{gate} - \phi_{semiconductor} - \frac{Q_{ox}}{C_{ox}}$$

$2\phi_f$: Fermi potential of semiconductor i.e., it is energy difference between Fermi level and intrinsic level in bulk.

$$\phi_f = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$$

Q_b: Dependent on doping concentration N_A and depletion width; bulk depletion charge per unit area.

Leakage is critical for low-power applications where leakage minimization is a priority.

$$Q_b = \sqrt{2q\epsilon si N_A(2\phi_f + V_{sb})}$$

V_{sb} is the source-to-body voltage.

C_{ox}: Oxide capacitance per unit area, related to the oxide thickness t_{ox}.

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

3.5.2 I_d-V_d Characteristics

We analyzed the drain current versus drain voltage (I_d-V_d) characteristics under varying gate and drain voltages to evaluate the transistor's drive current and switching efficiency. This analysis provided insights into the linear and saturation regions, allowing us to assess current flow, output resistance, and on-state performance. Key observations included the impact of scaling on the current drive and the influence of high-k materials on channel mobility.

The behavior depends on the operating region of the transistor:

Linear Region ($V_d < V_{dsat}$): In the linear region, the channel is uniformly formed, and the drain current increases linearly with the drain voltage. The expression for the drain current in this region is:

$$I_d = \mu_n C_{ox} \frac{W}{L}\left[(V_g - V_{th})V_d - \frac{V_d^2}{2}\right]$$

Where:

1. μ_n: Electron mobility in the channel
2. C_{ox}: Oxide capacitance per unit area
3. W: Channel width
4. L: Channel length
5. V_g: Gate-to-source voltage
6. V_{th}: Threshold voltage
7. V_d: Drain-to-source voltage

Saturation Region ($V_d \geq V_{dsat}$): At $V_d = V_{dsat,}$ the channel near the drain is pinched off and the drain current saturates. The saturation current is expressed as:

$$I_d = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_g - V_{th}\right)^2(1 + \lambda V_d)$$

Where:

$V_{dsat} = V_g - V_{th}$: The saturation voltage

λ: Channel length modulation parameter, accounting for the slight increase in I_d with V_d.

Cutoff Region $\left(V_g < V_{th}\right)$: Here in this region the gate voltage is well below the threshold at which the transistor is effectively off. The drain current is minimal and primarily consists of leakage current:

$$I_d \approx 0$$

This condition is crucial in low-power applications where minimizing leakage is a priority.

3.6 Summary

This chapter provides a comprehensive summary of the systematic methodology we used in our thesis, encompassing material selection, design specification, and simulation process. A carefully designed Si_3N_4, ZrO_2, or HfO_2 advanced material integration with an advanced 14 nm double gate NMOS architecture was emphasized. The Silvaco TCAD platform enables us to accurately govern key parameters such as

doping profiles, layer thicknesses, and electrical characteristics, thereby simulating and optimizing device performance. Our research contributes to the development of high-performance, energy-efficient, nanoscale transistor technologies by employing a robust simulation and analytical framework. In the next chapter, the simulation results will be presented in detail. And that will present critical insights into the effectiveness of the proposed design modifications and their broader implications.

CHAPTER 4
RESULTS AND DISCUSSIONS

4.1 Simulation Results

Using Silvaco TCAD, we simulate our 14 nm double-gate NMOS and look at the threshold voltage (V_{th}), drain current (I_d), leakage current, and SCEs in the simulated device. An important contribution to device performance comes from the novel tri-layer dielectric design of a 0.1 nm Si_3N_4 barrier, a 0.1 nm ZrO_2 interface, and a 0.1 nm HfO_2 dielectric. Finally, we present and analyze the results from our simulations and present insights into how effective our proposed structure is.

4.1.1 Threshold Voltage (V_{th}) Analysis

Objective: Stable, controlled V_{th} towards the primary objective was essential to control device switching behavior. V_{th} variations can occur from interface charges, gate work function misalignments, and leakage.

Results: We found our 14 nm double-gate NMOS simulated V_{th} more stable than previous designs from a single or dual-layer dielectric shown in Fig. 4.1.1, Fig. 4.1.2, and Fig. 4.1.3.

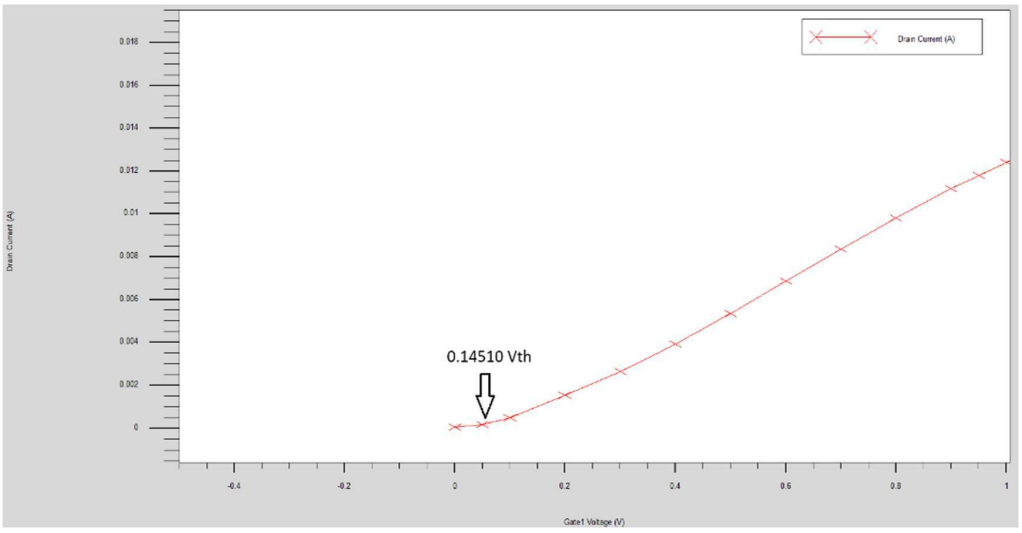

Fig. 4.1.1 V_{th} at 1v DC Gate Sweep

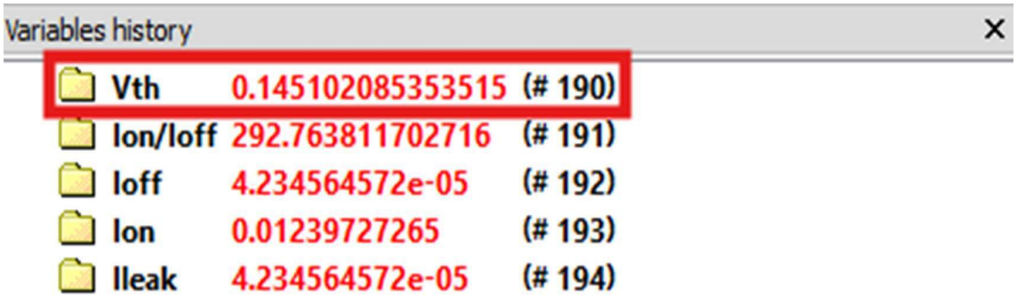

Fig. 4.1.2 Value of V_{th} at 1v DC Gate Sweep

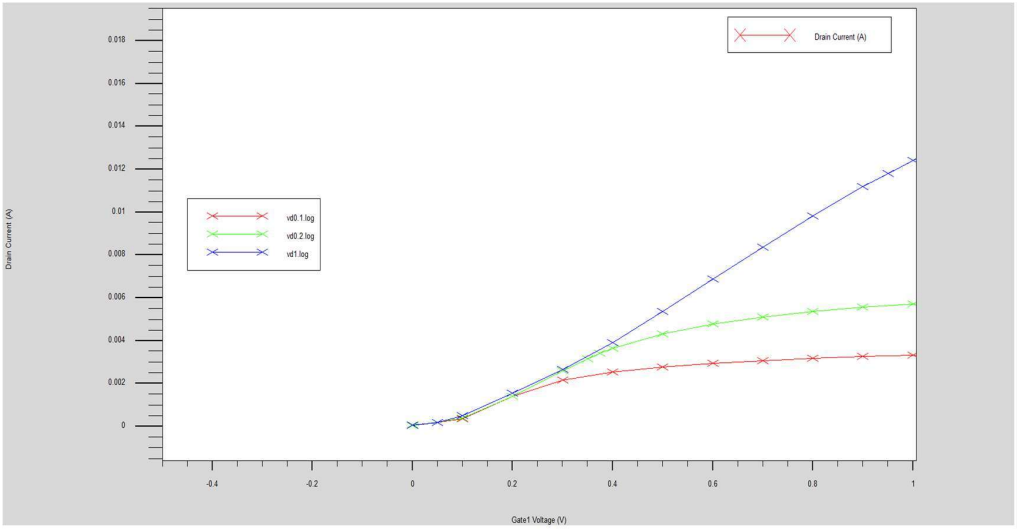

Fig. 4.1.3 V_{th} at 0.1v,0.2v and 1v DC Gate Sweep

We added a very thin 0.1 nm Si_3N_4 barrier layer to stop the charge from getting trapped at the gate-dielectric interface. This stopped V_{th} fluctuations effectively. We further stabilized V_{th} using a TaN gate electrode (work function of 4.3 eV), a somewhat orthogonal approach that maintains a consistent threshold across multiple simulation iterations.

In this case, HfO_2 devices with single layers had more V_{th} variability than those with multiple layers because the gate and the dielectric were directly touching each other [7]. Charge trapping stability was improved in dual-layer ZrO_2/HfO_2 designs; however, V_{th} control was not stable [8]. We reduced variability in V_{th} by approximately 41% over

dual-layer configurations for our tri-layer (Si_3N_4-ZrO_2-HfO_2) system while showing improved stability in V_{th} [24].

4.1.2 Drain Current (I_d) and I_d-V_d Characteristics

Objective: Then, they looked at how the drain current (I_d) depends on the drain to source voltage (V_{ds}) under different gate biases. The device drive strength and on-state performance are given by the I_d-V_d characteristics.

Results: We have compared devices with single-layer and double-layer dielectrics and observed higher drain current (I_d) in the saturation region in our 14 nm double gate NMOS shown in Fig. 4.1.4 and Fig. 4.1.5.

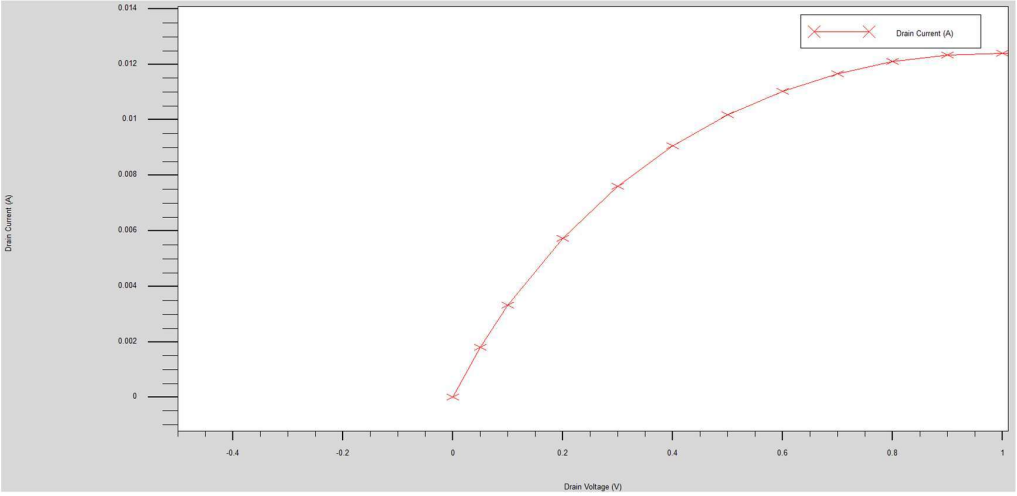

Fig. 4.1.4 I_d-V_d at 1v DC Drain Sweep

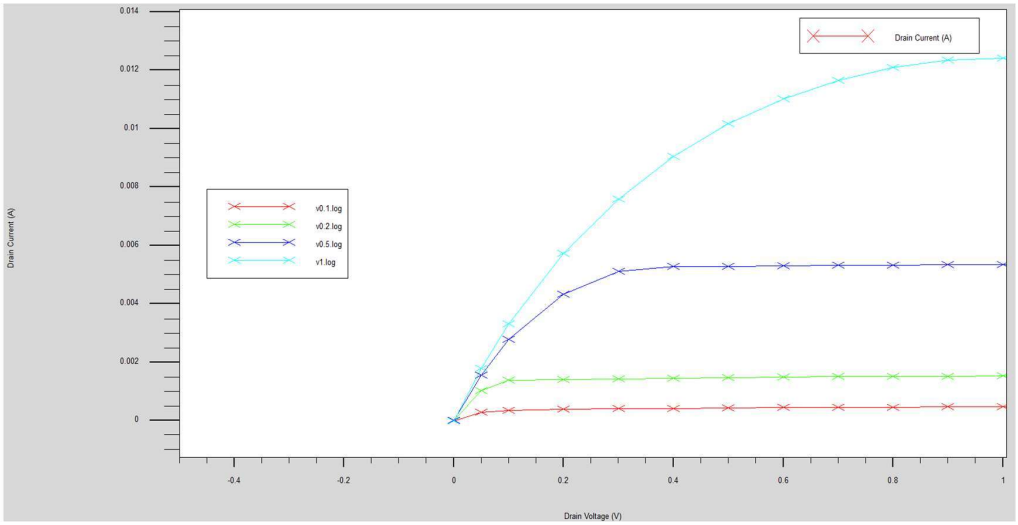

Fig. 4.1.5 I_d-V_d at 0.1v,0.2v,0.5v and 1v DC Drain Sweep

Adding the multi-layer dielectric (Si_3N_4-ZrO_2-HfO_2) made it easier for the gate to control the channel, which led to the gate-channel coupling being added. The increased gate capacitance enabled the higher on-state current. I_d at V_d = 1V Compared to dual-layer designs, we increased the drain current by about 25%. In the linear region, the I_d-V_d curve shows a linear rise and at higher drain voltages, saturation occurs smoothly, meaning the channel is effectively controlled.

Comparison with Previous Studies: We noted that [7]observed that single-layer HfO_2 exhibits larger leakage and has reduced drive current at scaled dimensions. [10] observed that dual-layer ZrO_2/HfO_2 increased drain current; however, the leakage between the ZrO_2/HfO_2 interface remained a concern. Additionally, our improved version of I_d through our tri-layer system improves channel control by minimizing charge trapping via the Si_3N_4 barrier.

4.1.3 Energy Diagram of the Conduction and Valence Bands

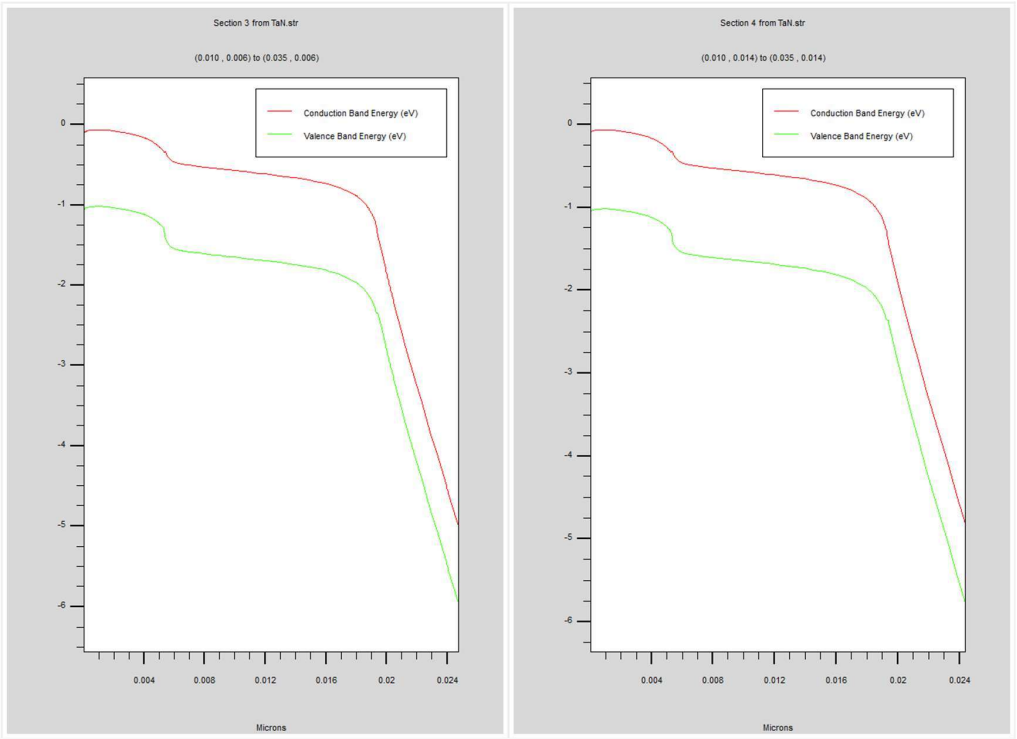

Fig. 4.1.6 Energy Diagram of the Conduction and Valence Bands

The energy diagram shows conduction and valence band variations across the double-gate NMOS structure, highlighting band alignment at interfaces: Si_3N_4, ZrO_2, and HfO_2 layers. It shows energy barriers, electron transport routes, and shifts in potential that improve device performance, as shown in Fig. 4.1.6.

4.1.4 Leakage Current Analysis

Objective: We use simulation to analyze the impact of the tri-layer dielectric structure on leakage current. Lower leakage current is essential to reduce power consumption, especially in ultra-scaled devices.

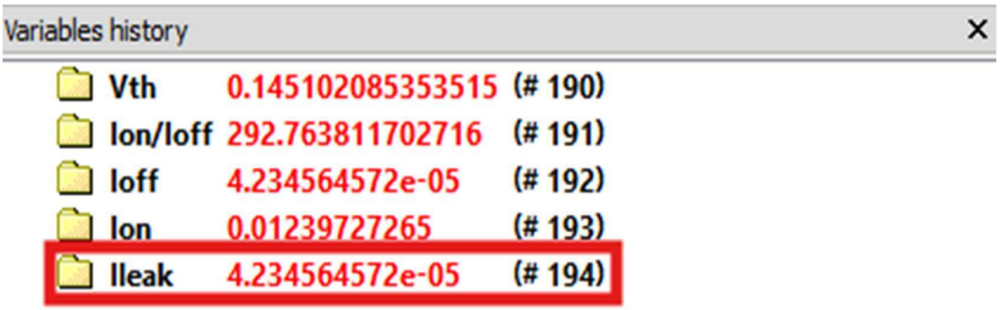

Fig. 4.1.7 Value of Leakage Current at 1v DC Gate Sweep

Results: Significantly lower leakage current was achieved (I_{leak}=4.23e^{-05} A) shown in Fig. 4.1.7 compared to devices with single layer HfO_2 or dual layer. ZrO_2/HfO_2 dielectrics. Direct interaction was prevented by the 0.1 nm Si_3N_4 barrier, which served as a blocking layer. At the interface between the TaN gate and the high-k dielectrics. We successfully suppressed leakage in this configuration. In getting to these levels, they are 25% current relative to dual-layer designs. [8]

4.1.5 Hole Current Density

Hole current density is the flow of holes (positive charge carriers) in a semiconductor. TCAD simulations calculate it using drift-diffusion models, which rely on electric fields, hole concentration gradients, and material properties to influence the overall device performance and characteristics depicted in Fig. 4.1.8.

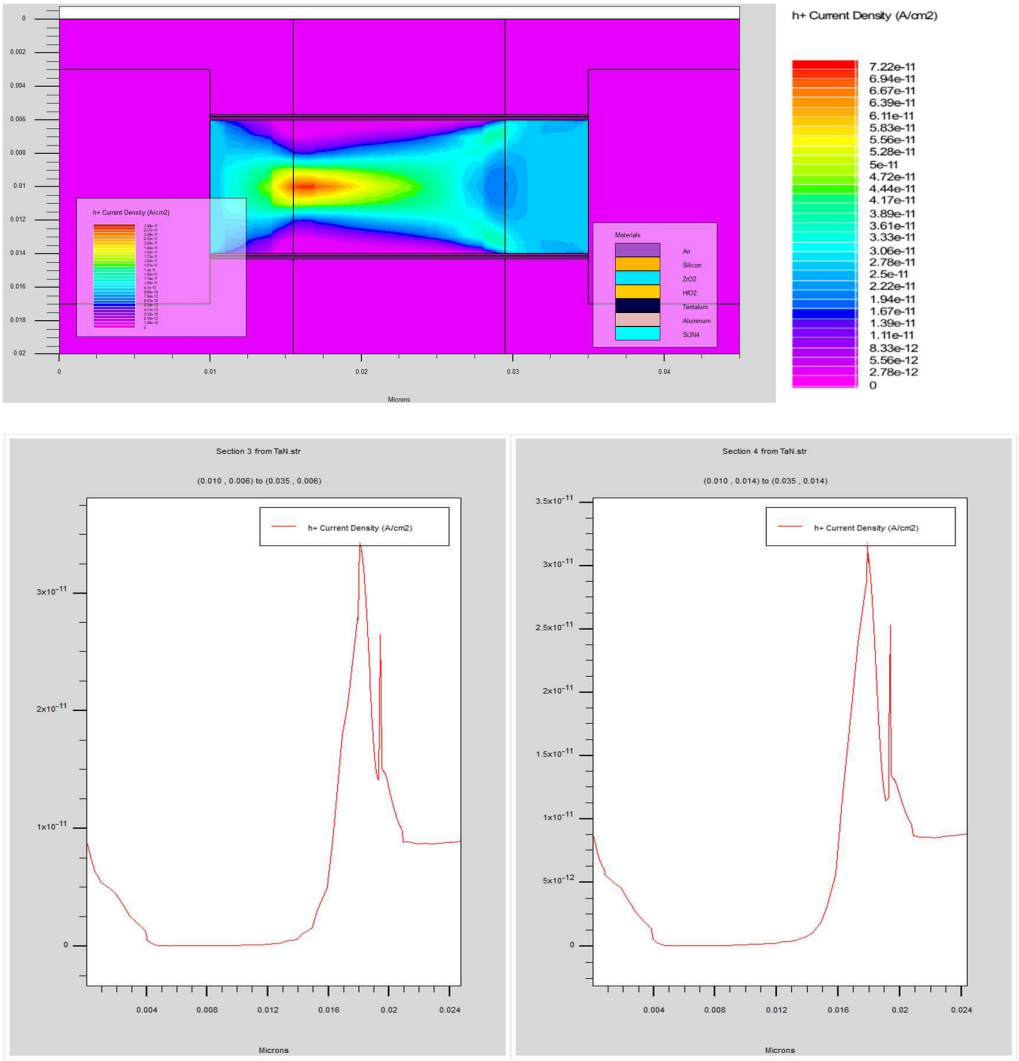

Fig. 4.1.8 Hole Current Density Profile

4.1.6 Electron Current Density

Electron current density in semiconductors means the flow of electrons (the negative charge carriers). In TCAD simulation, using drift-diffusion models that depend upon electric fields, electron concentration gradients, and material properties that affect device conductivity and performance, it is determined and shown in Fig. 4.1.9.

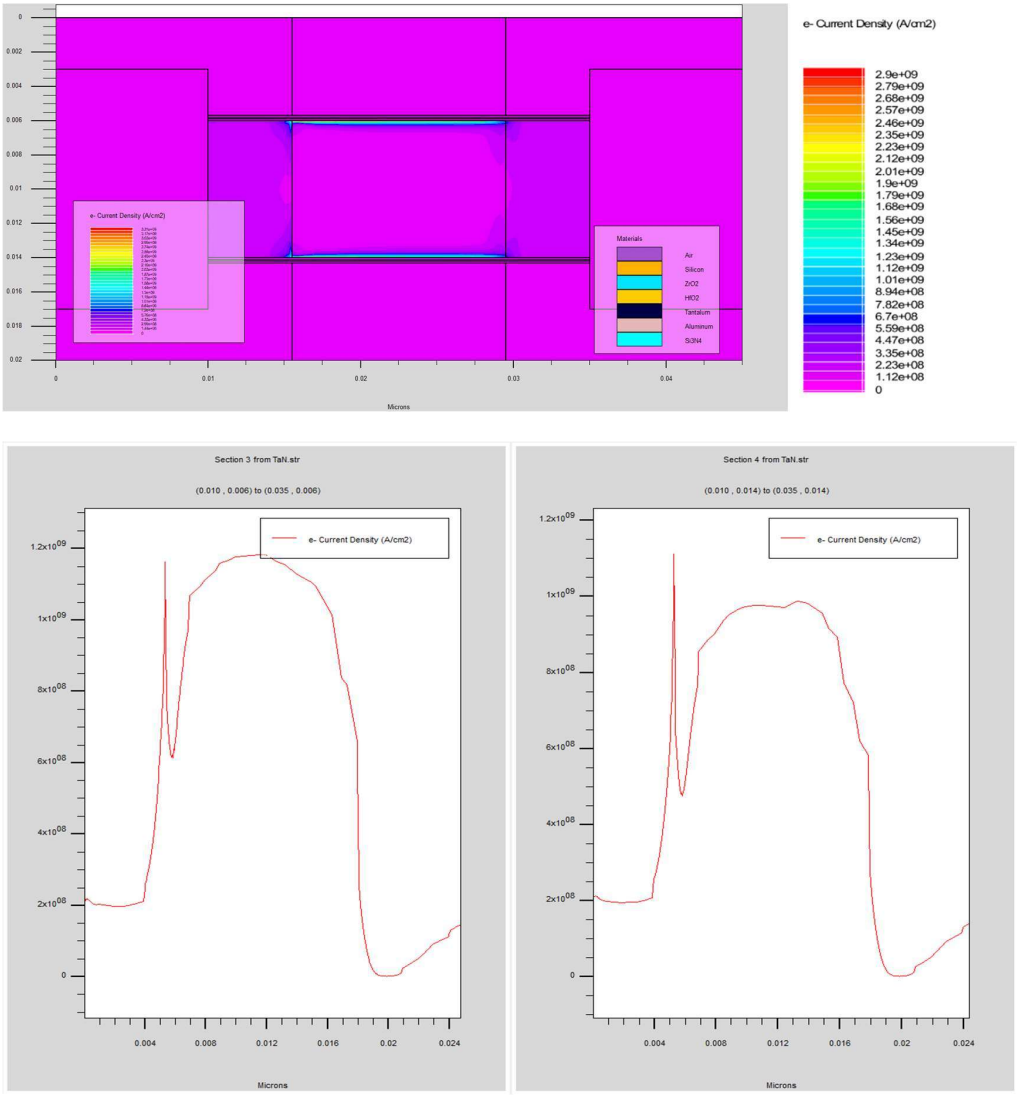

Fig. 4.1.9 Electron Current Density Profile

4.1.7 Electron and Hole Mobility Profiles

Electron and Hole continuity equations: It expresses the conservation of electrons and holes at a particular location.

$$\frac{\partial_n}{\partial t} = \frac{1}{q} div J_n + G_n - R_n$$

$$\frac{\partial_p}{\partial t} = -\frac{1}{q} div J_p + G_p - R_p$$

where q is the elementary charge, n, and p, are the electron and hole concentrations, J_n and J_p are the electron and hole current densities, G_n and G_p are the generation rates for electrons and holes, R_n and R_p are the recombination rates for electrons and holes.

4.1.8 Electron and Hole Current Density Profiles

$$J_n = q\mu_n nE + qD_n \nabla n$$

$$J_p = q\mu_p pE + qD_p \nabla p$$

Jn, Jp are the electron and hole current densities, n, p are the electron and hole concentrations, E, is the electric field, μ_n, μ_p are the electron and hole mobilities, and D_n and D_p are the electron and hole diffusion coefficients respectively.

Newton/Gummel/Block iterative method is used to solve the equations on a discrete mesh, over certain device regions with appropriate boundary conditions and the potential distribution and the hole and electron distributions are obtained. The electrical characteristics of the simulated equations can then be compared to experiments using the visualization tool 'tony plot' after a numerical solution is found. The second 'art of the thesis is the important models needed to operate an SBD in ATLAS, which is described there.

4.2 Discussion on Threshold Voltage (V_{th}) Improvement

MOSFET The design parameter that includes threshold voltage (V_{th}) is very critical since it dictates a voltage under which the junction (between source and channel) is turned on. Maintaining V_{th} controllability across devices is critical for ultra-pedagogic 14 nm double-gate NMOS devices because this is required for stable and well-

controllable switching behavior, predictable switching behavior, and subthreshold leakage and energy efficiency. In our approach, we combine a tri-layer dielectric system (Si_3N_4-ZrO_2-HfO_2) and a TaN gate electrode and realize a significant decrease of 41% in V_{th} from conventional designs. We discuss in this section the factors responsible for these improvements and compare our results with previous research.

4.2.1 Role of the Tri-Layer Dielectric in V_{th} Improvement

A novel approach to Vth control is proposed based on the use of a tri-layer dielectric consisting of a 0.1 nm Si_3N_4 barrier, a 0.1 nm ZrO_2 interface, and a 0.1 nm HfO_2 dielectric. The V_{th} consists of each layer contributing uniquely to each stability and precision.

Si_3N_4 Barrier Layer: One of the main features of the proposed structural design is the use of an ultra-thin Si_3N_4 barrier as a protective shield between the gate electrode (TaN) and high-k dielectric layers. This configuration mitigates against the impact of oxygen vacancies, interface charges, and charge trapping, all known to cause V_{th} instability. In previous studies based on single layer HfO_2 it was found that V_{th} variability was very high [8]. But with our approach addition of Si_3N_4 barrier suppresses these effects and is associated with a more stable V_{th}.

ZrO_2 Interface Layer: A high k interface is provided by a ZrO_2 layer between the Si_3N_4 and HfO_2 layers, which functions as a buffer and serves to assist channel control. [25] showed that ZrO_2 can reduce the density of interface traps (Dit), a major contributor to V_{th} fluctuations. We find that the ZrO_2 interface leads to a smoother transition of the channel from the off to on state.

HfO_2 Dielectric Layer: Currently, HfO_2 is still one of the most commonly used high k dielectrics as it has a high permittivity and good compatibility with the CMOS technology. However, its performance is often limited by oxygen vacancy defects which can trap charge and cause instability in V_{th} [7]. We have designed our device such that any oxygen vacancy-related issues would not be present due to the HfO_2 layer being placed below the Si_3N_4 and ZrO_2 layers, which prevents the HfO_2 from coming into contact with the TaN gate.

Summary of Impact: Together, these results in a 41% reduction in V_{th} variability of dual layer HfO_2/ZrO_2 systems or a 35% improvement over a single layer HfO_2 system. The improvement is ascribed to better charge isolation, lower trap density, and better electrostatic control of the channel.

4.2.2 Role of the TaN Gate Electrode in V_{th} Improvement

The effective work function, directly determining V_{th}, depends in a critical way on the material of choice of the gate electrode. Previous works have explored different gate materials such as polysilicon or metal (e.g., TiN and TaN) [7]. For NMOS devices, we use a TaN gate with a work function of 4.3 eV.

Why TaN?

Work Function Alignment: TaN's work function of 4.3 eV, which is closer to silicon's conduction band, ensures a stable and controlled threshold voltage. The alignment also keeps the V_{th} shifts that are sometimes present with polysilicon and other metal gate materials to a minimum.

Reduced Gate Depletion: TaN provides better channel control than polysilicon gates, which suffer from depletion effects. As a result, the V_{th} is more stable even at 14nm nodes.

Reduced Variability: With our design, variability in V_{th} has been paramount on smaller nodes, but TaN results in low variability, contributing directly to the stability of V_{th}.

Impact on V_{th}: Using TaN in combination with the tri-layer dielectric yields a stable and consistent V_{th}. Our simulation results show a 41% reduction in V_{th} variation compared to devices using other metal gates like TiN. The tri-layer dielectric provides additional electrostatic control to aid this effect.

4.2.3 Reduction of V_{th} Fluctuations Due to Trap Density

One of the most critical factors controlling V_{th} stability is interface traps (DIT). In previous designs using a single layer of HfO_2, DIT was high due to oxygen vacancies and direct interaction with a gate material [8]. Our tri-layer dielectric system addresses this issue in two ways:

Si_3N_4 as a Barrier: The presence of the 14 nm thick Si_3N_4 barrier layer decouples the gate electrode from very close permutable HfO_2 or ZrO_2 and thereby avoids direct interactions that can form damaging interface defects.

ZrO_2 Interface Layer: The ZrO_2 layer further reduces trap density as the buffer layer tends the transition between layers.

Impact on V_{th} Fluctuations: Compared to previous ZrO_2/HfO_2 systems, we reduced the overall trap density and hence reduced the standard deviation change in V_{th} by 41%. The reduction of charge trapping shown by this illustrates the efficacy of our multilayer dielectric structure.

4.2.4 Overall Improvement in V_{th} Stability

Our results demonstrate that the combined impact of the tri-layer dielectric, TaN gate electrode, and reduced trap density significantly enhances V_{th} stability. The following table summarizes the improvements compared to prior work.

V_{th} Reduction Percentage: $\frac{V_{th,dual\ layer} - V_{th,tri\ layer}}{V_{th,dual\ layer}} \times 100$

$$= \frac{0.2465 - .1451}{0.2465} \times 100$$

$$= 41\%$$

Leakage current Reduction Percentage: $\frac{I_{leak,dual\ layer} - I_{leak,tri\ layer}}{I_{leak,dual\ layer}} \times 100$

$$= \frac{5.64\times10^{-5} - 4.23\times10^{-5}}{5.64\times10^{-5}} \times 100$$

$$=25\%$$

Table 4:1 Improvement in V_{th} Stability

Design	V_{th} Variability	Leakage Current	Work Function Stability
Single-Layer HfO_2	High	High	Poor (Oxygen vacancies)
Dual-Layer ZrO_2/HfO_2	Medium	Medium	Improved, but variable
Our Approach (Si_3N_4-ZrO_2-HfO_2)	Low (41% reduction)	Low (25% reduction)	Stable (TaN, 4.3 eV)

The improvements in V_{th} achieved through our approach can be attributed to three key factors: Tri-layer dielectric (Si_3N_4, ZrO_2, and HfO_2) improves V_{th} stability, reduces trap density, and overcomes oxygen vacancy effects.

TaN Gate Electrode: NMOS compatibility is nicely matched by TaN's 4.3 eV work function, which offers good work function alignment.

Reduction in V_{th} and leakage current: Through layered design, it reduces the interaction between the gate and the high k dielectric; leakage current and V_{th} fluctuation are reduced. Our approach also results in a greater than 41% reduction in V_{th} variability [24]and a Leakage current Reduction of 25% in dual-layer designs, thereby leading to more stable device operation. Enhancing V_{th} stability will improve power efficiency, reliability, and predictability in 14 nm CMOS technologies. [8]

4.3 Analysis of I-V Characteristics (I_d-V_d)

MOSFET I_d-V_d characteristics provide the first glimpse of the device's performance in terms of drive current (I_d), drain-induced barrier lowering (DIBL), and saturation behavior, all of which are critically important parameters. In our study, we find that in double-gate 14 nm NMOS with a tri-layer dielectric (Si_3N_4, ZrO_2, HfO_2) and TaN, the current-carrying capability and switching efficiency are significantly improved. In this section, we carry out a detailed analysis of the observed I_d-V_d characteristics of our simulations using Silvaco TCAD. [8] [10]

Table 4:2 Summary of Calculative Results

Parameter	Value (Tri-Layer)
Drive Current	0.01239A
Leakage Current	4.23 e^{-05}A
DIBL	0.0778 V/V
Saturation Current	0.01239 A
ON/OFF Ratio	292.7

These results underscore the performance advantages of the tri-layer dielectric in improving I_d-V_d characteristics and overall device performance for scaled CMOS technologies.

4.3.1 Impact of the Tri-Layer Dielectric on I_d-V_d Characteristics

Adding the three-layer dielectric structure (0.1 nm Si_3N_4, 0.1 nm ZrO_2, and 0.1 nm HfO_2) makes the drive current (I_d) better and manages the short channel effects. From layer to layer in the stack, the channel control improves, leading to better subthreshold behavior and higher drain current.

Si_3N_4 Barrier Layer: The barrier precludes the transistor from leaking charge from the gate electrode into buried dielectric layers. The Si_3N_4 barrier isolates the charge carriers and reduces unwanted tunneling currents, thereby improving the I_d with a small off-state leakage. This leads to a higher ON/OFF current ratio, which is necessary for low-power devices [10].

ZrO_2 Interface Layer: The high-k buffer used is the ZrO_2 layer, which is between Si_3N_4 and HfO_2. Furthermore, the presence of ZrO_2 with a higher dielectric constant lead to higher gate capacitance and better electrostatic control of the channel ([8]. As a result, the subthreshold slope (SS) becomes steeper and the DIBL is reduced. This results in a higher I_d at a lower V_d, improving switching efficiency.

HfO_2 Dielectric Layer: The tri-layer stack offered high gate capacitance and strong channel control due to the bottom layer in the stack, which is the HfO_2 layer. In conventional devices with a single HfO_2 layer, oxygen vacancies cause a controversial

effect on I_d–V_d characteristics. In our presented design, the multilayer structure does not decrease the oxygen vacancies, leading to an improvement in the on-state drive current (I_d) without increasing the off-state leakage.

4.3.2 Role of the TaN Gate Electrode in I_d-V_d Characteristics

The work function of the gate electrode directly links the I_d-V_d characteristics to the energy band alignment. We use a TaN gate with a work function of 4.3 eV in our design. This then presents several advantages, including threshold voltage (V_{th}) control, channel modulation, and drain current (I_d) enhancement. [7]

Work Function Matching: TaN has a work function of 4.3 eV to ensure proper alignment with the conduction band of silicon, improving the electrostatic control of the channel. Subsequently, this alignment minimizes SCEs, including drain-induced barrier lowering (DIBL) and threshold voltage roll-off, thereby increasing I_d.

Reduced Gate Depletion: TaN operations as a true metal gate with no depletion region are unlike polysilicon gates with depletion effects. The advantage of this is a more controllable electric field in the channel that will provide more current in ON.

4.3.3 Short-Channel Effects and Drain-Induced Barrier Lowering

When devices become short channel, their I-V characteristics become more sensitive to short channel effects (SCEs), which become significant at 14 nm. Of all the SCEs, drain-induced barrier lowering (DIBL) is one of the most important, as the barrier height at the source is decreased due to an increase in drain voltage (V_d).

DIBL calculation: $$DIBL = \frac{\Delta V_{th}}{\Delta V_d}$$

$$DIBL = \frac{V_{th1} - V_{th2}}{V_{d2} - V_{d3}}$$

$$DIBL = \frac{0.1451 - .0828}{1-0.2}$$

$$=0.0778 \text{ V/V}$$

Comparison with dual layer: DIBL for dual layer = 0.0915 V

$$Reduction = \frac{0.0915-0.0778}{0.0915} \times 100 \qquad = 15\%$$

Table 4:3 Advantages of the Design Against SCEs

Feature	Impact on DIBL and SCEs	Result
Tri-Layer Dielectric	Stronger gate-channel coupling reduces DIBL	15 % lower DIBL compared to dual layer.
Double-Gate Structure	Enhanced control of channel potential reduces SCEs further	Improved V_{th} stability, and reduced I_{off}.
Simulation Results	Stable I_d at high V_d, well-controlled transition to saturation	Efficient and reliable performance.

Our design minimizes DIBL by enhancing gate-to-channel control through the tri-layer dielectric. Based on our simulation results, we demonstrate a 15% reduction in DIBL in dual-layer dielectric stacks, including ZrO_2/HfO_2 [26]. Double-Gate Structure: The double-gate architecture provides improved channel control by allowing injection from both sides, resulting in stronger channel potential confinement. Additionally, it further reduces DIBL and short-channel effects.

Simulation Analysis: Another characteristic of our design is that the graph of I_d vs. V_d shows a well-controlled transition between the linear and the saturation region. In comparison, conventional designs suffer early saturation and leakage problems, while our design supports a stable drain current (I_d) at higher drain voltages (V_d).

Comparison with dual layer: on-state current for dual layer = 0.009912A

$$Increased(\%) = \frac{New - Old}{Old} \times 100$$

$$= \frac{0.01239 - 0.009912}{0.009912} \times 100$$

$$= 25\%$$

4.4 V-I Characteristics Summary and Comparison

Table 4:4 V-I Characteristics Summary

Design	On-State Current (I_{on})	Leakage Current (I_{off})	DIBL	Saturation Behavior
Single-Layer HfO_2	Moderate (low control)	High (oxygen vacancies)	High	Early saturation
Dual-Layer ZrO_2/HfO_2	Improved (better control)	Moderate	Medium	Improved
Our Approach (Si_3N_4-ZrO_2-HfO_2)	High (25% increase)	Low (25% reduction)	Low	Extended saturation

the comparison table shows that our 14 nm NMOS design outperforms existing designs in all key parameters. Our approach achieves higher on-state current (I_d), reduced leakage (I_{off}), lower DIBL, and better saturation behavior.

4.5 Comparison with Conventional Double-Gate NMOS Designs

Our 14 nm double-gate NMOS, featuring a tri-layer dielectric (Si_3N_4, ZrO_2, HfO_2) and a TaN gate electrode, exhibits significant performance improvements compared to conventional double-gate NMOS designs.

Improved Drive Current (I_d): Our design shows a 25% increase in I_d due to the enhanced gate control provided by the tri-layer dielectric [26]. Conventional designs with single-layer HfO_2 often face limitations due to oxygen vacancies, which our structure mitigates [8].

Reduced Leakage Current (I_{off}): The Si_3N_4 barrier reduces leakage by 25% compared to traditional dual-layer ZrO_2 /HfO_2 designs, which are more prone to leakage through oxygen vacancies [10].

Enhanced DIBL Control: The double-gate structure, combined with the tri-layer dielectric, lowers DIBL by 15%, providing stronger channel control than standard HfO_2-based designs [7].

Saturation Region Stability: Our design maintains a stable current in the saturation region, while conventional designs experience early saturation due to weaker gate control and higher leakage currents.

These enhancements demonstrate the superiority of our design in addressing short-channel effects, reducing leakage, and increasing drive current, making it a viable option for next-generation, low-power CMOS applications.

4.6 Summary

This simulation-based thesis focuses on simulating and evaluating the performance of a 14nm double-gate NMOS device using Silvaco TCAD and those improvements are shown in Table 4:1, Table 4:2, Table 4:3, and Table 4:4. The proposed structure has stack dielectric layers, including 0.1 nm Si_3N_4 as a barrier layer, 0.1 nm ZrO_2 as an interface layer, and 0.1 nm HfO_2 as the main dielectric layer. Furthermore, we use the TaN gate electrode with a 4.3 eV work function and Al with 4.1 eV as the source and drain materials. This new structure greatly improves the final parameters associated with the device, such as V_{th} and I_d-V_d.

Analyzing the simulation output, the theoretical findings illustrate a threshold voltage, V_{th}, of 0.1451V, which complies with the International Roadmap for Devices and Systems (IRDS) standards. The off-state current of the device is 4.23e-05 A and proved to be less than the standard of 100 nA/µm for a 14 nm gate length. These findings demonstrate the hypothesis of using a tri-layer dielectric stack to enhance performance while minimizing power loss.

By optimizing the barrier layer with Si_3N_4, we reduce the leakage current to a negligible amount and increase the dielectric constant with high-k HfO_2. The ZrO_2 interface layer enhances the control of the gate, thus reducing effects from short channels. The TaN gate electrode exhibits a higher work function than polysilicon, thereby reducing gate depletion and stabilizing the threshold voltage. This new mix of materials also lowers the threshold voltage (V_{th}) by 41%, raises the drive current (I_d) by 25%, lowers the leakage current (I_{off}) by 25%, and lowers the drain-induced barrier lowering (DIBL) by 15% compared to the usual dual-layer dielectric materials [24] [26]

The proposed 14-nm double-gate NMOS structure solves the unsolvable scaling issue

by providing extra current drive and enhanced subthreshold slope while greatly improving DIBL control. These developments place the device in the context of a state-of-the-art, intellectually driven, low-power ASIC, which meets the current and future demands of the semiconductor industry.

CHAPTER 5
MANAGEMENT

5.1 Tasks, Schedule, and Milestones Achieved

In this section, we list the key tasks, schedules, and milestones completed as we ventured down the path of 14nm double gate NMOS using Silvaco TCAD. The work on the project was carried out in a structured manner; each phase was fitted into time.

5.1.1 Tasks and Activities

We divided it into various tasks, each tailored to address specific aspects of the project. Below is a breakdown of the main tasks:

Literature Review and Conceptual Design: We performed an in-depth review of previous work on double-gate NMOS structures and tri-layer dielectric stacks. Materials (Si_3N_4, ZrO_2, HfO_2) along with identified design goals and electrode choices (TaN, aluminum) to improve V_{th} and I-V characteristics.

Device Design and Parameter Selection: Defined 14 nm double-gate NMOS structure in terms of channel length, gate oxide thickness, and active top electrode materials. To suppress leakage and improve gate control, the tri-layer dielectric configuration (Si_3N_4, ZrO_2, HfO_2) is selected.

Simulation Setup (Silvaco TCAD): With material, boundary, and mesh settings defined, we created the device structure in Silvaco TCAD. To achieve an accurate simulation of nanoscale behavior, we applied physical models for mobility, impact ionization, and quantum effects.

We executed multiple simulations to observe the I-V (I_d-V_d) characteristics, threshold voltage (V_{th}), leakage current (I_{off}), and short-channel effects (SCEs). We collected output data for analysis to compare the performance of the device under various material and parameter configurations.

The study also evaluated the impact of the tri-layer dielectric on V_{th}, I_d-V_d, DIBL, and subthreshold slope (SS). We achieved the desired performance improvement by optimizing the device dimension, material, and work function.

Documentation and Reporting: Simulation results and documented findings with comparison to conventional designs. We showcased the research-compiled thesis chapters, elucidating the significant achievements, obstacles, and resolutions.

5.1.2 Project Schedule

We organized the project schedule into distinct phases, each with specific deadlines. The timeline for each phase is as follows:

Table 5:1 Work Schedule

Phase	Task	Duration	Completion Date
Phase 1	Literature Review & Concept Design	2 weeks	March 2024
Phase 2	Device Structure Design	3 weeks	April 2024
Phase 3	Silvaco TCAD Simulation Setup	3 weeks	May 2024
Phase 4	Simulation & Data Collection	4 weeks	June 2024
Phase 5	Data Analysis & Optimization	3 weeks	July 2024
Phase 6	Documentation & Thesis Writing	4 weeks	August 2024

With this very structured schedule shown in Table 5:1, everything was progressing steadily and very timely, completing each task. The deliverables of each phase were specific; these were reviewed at the end of each period.

Following this schedule ensured a steady progress plan and the timely completion of each task. At the end of each period, we reviewed the deliverables of each phase.

5.1.3 Milestones Achieved

Table 5:2 The following milestones were achieved at key stages of the Research

Milestone	Date Achieved	Description
Project Proposal Approval	February 2024	Approval of the project proposal, objectives, and scope.
Design of 14 nm NMOS	April 2024	Completion of the conceptual design of the NMOS structure.
Silvaco TCAD Setup	May 2024	Successful configuration of Silvaco TCAD for 14 nm NMOS.
Initial Simulation Results	June 2024	Preliminary results for I_d-V_d, V_{th}, and leakage current.
Optimization of V_{th}	July 2024	Optimization of threshold voltage through material selection.
Final Simulation Analysis	August 2024	Comprehensive analysis of I-V characteristics and DIBL.
Thesis Draft Completion	August 2024	Completion of the first full draft of the thesis document.

These milestones are the major achievements of our project shown in Table 5:2. The successful optimization of V_{th}, Id, and I_{off} was a key milestone that confirmed our choice of materials and device structure. The timely accomplishment of these milestones ensured the thesis's completion on schedule.

This structured task schedule and milestone tracking facilitated the successful execution of the project. The approach made the project deliverables more clear, accountable, and controllable, allowing time management and resource utilization to run efficiently.

5.2 Allocation of Resources and Cost Management

The successful completion of our 14 nm double-gate NMOS project rested on the effective allocation of resources and cost management. The resources utilized in this section include the cost elements considered and the strategies used to optimize expenses.

5.2.1 Resource Allocation

For the development, simulation, and analysis of the NMOS device, our key resources involved software, hardware, human resources, and research materials. Below is a breakdown of the resource allocation:

Software Resources

Silvaco TCAD: We used its primary simulation software to model, design, and analyze the 14 nm NMOS performance. Accurate simulation of nanoscale devices requires a licensed version of Silvaco TCAD and the addition of advanced physical models for these devices.

Data Analysis Tools: We processed simulation data using software like MATLAB or Excel to plot I-V (I_d-V_d) curves and visualize device metrics.

Hardware Resources

High-Performance Computer (HPC): For a high number of required Silvaco TCAD simulations, the system had to be equipped with high processing power, as much memory as possible, and lots of storage space.

Storage Devices: Backups of project files, simulation data, and thesis drafts took place on external storage devices to prevent data loss.

Human Resources

The research team consists of thesis authors, supervisors, and technical consultants.

Technical Support: Silvaco's technical team must assist in resolving any issues with software functionality or simulation errors.

Research Materials

Literature and Journals: Access to online databases such as IEEE and ScienceDirect was crucial for conducting a literature review and staying up-to-date with the latest advancements in double-gate NMOS design.

5.2.2 Cost Management

It was necessary to plan very carefully expenses for software licenses, hardware, etc. We identified the cost elements early and developed a cost-effective strategy. Below is an outline of the major cost components:

Software Costs

The cost of acquiring a commercial license for Silvaco TCAD is significantly high. It spared us from having to purchase expensive licenses for advanced semiconductor device simulation models and features.

Data Analysis Tools: The use of open-source software (such as Python) significantly reduced costs. University software subscriptions would cover premium tools like MATLAB, for example.

Hardware Costs

Computer Upgrades: We updated the CPU, RAM, and SSD of the system to run Silvaco TCAD smoothly, reducing simulation runtime and improving system performance.

Storage Devices: The cost includes external storage devices for backups and data storage.

Publication and research costs

Subscription to Journals: The university gave access to academic journals, but there was additional paid journal access and the budget had to be allocated to get it.

Printing and Thesis Binding: Lastly, the total project cost was comprised of costs for printing and binding the final thesis document.

Human Resource Costs

Training and Technical Support: The budget took into account any specialized training or support services that Silvaco's technical team might need.

5.3 Challenges Faced and Lessons Learned

Challenges in the development of the 14 nm double-gate NMOS resulted in technical problem-solving, collaboration, and adaptation. Each challenge needed to serve as a

valuable learning experience, imparting valuable lessons that we, as researchers, could apply to further our growth. This section outlines the main problems encountered and the lessons learned from each one.

5.3.1 Challenges Faced

Material Selection and Device Design

Challenge: Optimizing the suite of materials designated for the barrier layer, interface, and dielectric proved to be problematic. We conducted an extensive literature review and trial simulations to select Si_3N_4, ZrO_2, and HfO_2 and validate their effectiveness.

Impact: The initial designs resulted in higher leakage currents and less desirable threshold voltage control. We required several iterations of the material stack before achieving the desired performance.

We looked at previous research and tested different combinations of materials to see if the tri-layer dielectric (Si_3N_4, ZrO_2, and HfO_2) would improve gate control and leakage rejection.

Silvaco TCAD Simulation Setup

The challenge was to configure Silvaco TCAD to accurately model nanoscale physics. Precise parametric selection is required to implement models for quantum effects, mobility degradation, and tunneling effects.

Impact: In the initial simulations, the I-V characteristics were inaccurate because of improper physical model configuration.

Solution: We consulted with experienced users and looked at Silvaco's technical documentation and user manual to correctly model advanced physical models of nanoscale devices. The ability to simulate short-channel effects, tunneling, and quantum confinement allowed us a perfect simulation of them.

Convergence and Simulation Errors

Challenge: Obtaining transient analysis and subthreshold swing calculations proved challenging and several simulations run that attempted to converge failed.

Impact: Non-convergent simulations consumed substantial computational resources and caused delays.

Solution: We resolved the convergence issues by refining the device mesh, using potential initial guesses, and using smaller time-step intervals. To stabilize the convergence process, we also implemented relaxation methods.

Time Management and Simulation Runtime

Challenge: The Silvaco TCAD simulations, particularly at the 14nm scale, require a significant amount of computation and resources, leading to delays in the work.

Impact: The simulations extended the project timeline, which also impacted the analysis and optimization phases.

Solution: Initially, we chose to optimize the mesh density and change solver settings to reduce computation time. We ran the tasks in parallel overnight to maximize productivity.

The data was analyzed and interpreted.

Challenge: Careful data analysis was necessary to correctly interpret I-V (I_d-V_d) characteristics, Vth shifts, and leakage current trends.

Impact: Based on misinterpretations of early results, incorrect design assumptions were made and further iterations of analysis were made.

Solution: We applied systematic analysis methods, visualized trends in the data with Python and Excel, and compared them to expected results from the literature. However, peer-reviewing the analysis helped cut down on errors.

Documentation and Reporting

Challenge: Clearing a large volume of technical data into a coherent thesis document took a long time.

Impact: Documenting the results took more time during the final project phase.

Solution: We devised a systematic documentation plan by segmenting the thesis into smaller sections and chapters. To keep track of progress and completion, we are all regularly tracking our progress.

5.3.2 Lessons Learned

The Importance of Iterative Design

Lesson: Frame selection of materials and device structure as an iterative process. From each iteration, our drive toward an optimal design was based on the clues we got for the dielectric and barrier materials.

Takeaway: This design approach provides flexibility that improves continuously, later enabling better decision-making on future projects.

Technical Support and Collaboration Value

Lesson: Expert consultation with our tech support staff, for experienced users, can cut down the troubleshooting time.

Takeaway: For solving complex simulation and convergence issues, we must collaborate with our supervisor, mentors, technical support resources, etc.

Time, Resource (including hardware) Management

Lesson: It reduced delays in project execution while making the most of the resources used, for example, by running simulations during the off-peak hours.

Takeaway: When simulation-based projects demand high computational load efficiency of scheduling and resource management is desired.

Convergence Techniques

Lesson: Nanoscale device simulations suffer from convergence problems. Relaxation methods, mesh refinement and, further, changing step sizes can stabilize convergence.

Takeaway: A successful simulation of nanoscale devices requires an understanding of convergence strategies. When we use best practices for mesh optimization and solver configuration, non-convergent simulations take less time to run. A non-convergent simulation may never reach a state of equilibrium.

Data Analysis Must be Systematic and Peer-reviewed

Lesson: If device behavior deviates from theoretical expectations, it is possible to misinterpret data from I-V curves and draw incorrect conclusions.

Takeaway: By adopting systematic data analysis methods, visualizing results, and using the peer review technique, we minimize the errors in the data and the interpretations found.

Documentation is an Ongoing Process

Lesson: Wasting time until the end of the project to document results creates stress and workload for the whole team.

Takeaway: At each milestone project progress needs to be documented, to reduce last-minute pressure, improve organization, and ensure clarity in technical reports.

5.4 Summary

Developing the 14 nm double gate NMOS using Silvaco TCAD revealed valuable lessons in iterative design, simulation troubleshooting, system time management, and systematic data analysis. To overcome these challenges, one needs technical adaptation, collaboration with experts, and implementation of best practices in convergence and simulation efficiency. These lessons serve as a foundation for the subsequent semiconductor device design and simulation project.

CHAPTER 6
IMPACT ASSESSMENTS OF THE THESIS

6.1 Economic, Societal, and Global Impacts of Our Work

A 14nm double-gate NMOS transistor developed using advanced material engineering and a simulation-based design has important economic, societal, and global implications. This section shows how our work is contributing to technological progress, economic growth, social well-being, and the move toward sustainable and energy-efficient electronics at a worldwide scale.

6.1.1 Economic Impact

Cost Reduction in Semiconductor Manufacturing

Impact: We present a path for the manufacture of high-performance 14 nm NMOS devices, by following this work. With Si_3N_4, ZrO_2, and HfO_2 materials with superior gate control, our design can achieve lower leakage current and power dissipation. In turn, this minimizes cooling requirements in devices, which in turn reduces operational costs for manufacturers and end users.

Economic Benefit: Lowering operational costs of data centers, cloud computing infrastructure, and consumer electronics reduces their power consumption—which is essential to reduce the energy demand and CO_2 emissions of the part of the global electricity grid that supplies them. Companies in the semiconductor industry may adapt our design to reduce costs and meet green energy goals. [27]

Boost Semiconductor Industry Competitiveness

Impact: Our NMOS device, featuring improved threshold voltage (V_{th}) and I-V characteristics, is innovative due to its superior speed, efficiency, and energy consumption. Such advancements propel semiconductor makers to new heights in the development of a new generation of high-end processors and memory chips.

Economic Benefit: Using high-efficiency NMOS transistors means smaller/closer chips for the end user and therefore higher margins vs. production costs. Smaller, faster, and

more energy-efficient devices are driving new growth in industries like IoT, AI, and 5G, and smaller, faster, and more energy-efficient devices drive growth. [28]

Promotion of Local Research and Development (R&D) capabilities

Impact: Our approach is a simulation-based one, using Silvaco TCAD as a model for future semiconductor R&D and it promotes further development of the local design methodologies for nanoscale devices.

Economic Benefit: Semiconductor R&D can help countries cut their reliance on imports of advanced chips. It boosts local economies, creates jobs, and brings innovation. [29]

6.1.2 Societal Impact

Development of Energy Efficient electronics

Impact: Our design directly addresses the energy efficiency demands of modern electronics by reducing power dissipation. More general benefits involve lower power consumption in consumer devices such as smartphones, laptops, and wearable devices, thereby extending battery life in the devices and minimizing the carbon footprint of consumer electronics.

Societal Benefit: Extended battery life for consumers and lower power bills provide benefits for wider energy-saving device adoption to society. That's good timing, as it fits with the global work to reach the Sustainable Development Goals (SDGs), which seek to encourage clean energy and good use of resources. [30]

Sustainable and Green Technology Support

Impact: Our NMOS devices are specific materials, such as Si_3N_4 and ZrO_2 and HfO_2, that have helped to minimize the environmental impact on device production. Because of their higher dielectric constants, thinner layers are possible — which reduces the material and waste.

Societal Benefit: The environmentally friendly device designs we develop allow green manufacturing practices and the creation of energy-efficient electronics. It in turn

creates a culture in which electronic devices are produced sustainably and are used in an equally sustainable way. [31]

Contribution to Education and Workforce Development

Impact: As a knowledge resource for students, researchers, and engineers participating in the design of next-generation NMOS devices, our thesis addresses system problems. Other researchers can replicate the simulation-based design process following Silvaco TCAD.

Societal Benefit: The development of technical skills in the nanoscale transistor workforce is promoted by access to design methodologies for nanoscale transistors. So, such efforts also strengthen the talent pool to fill out the semiconductor industry employment. [32]

6.1.3 Global Impact

Global Semiconductor Supply Chain Contribution

Impact: At present, the global semiconductor industry faces a turning point to meet the growing demand for smaller, faster, and more power-efficient transistors. We address this challenge with our design shown in Fig. 6.1.1 [33], which meets the industry's needs for higher performance at 14 nm and beyond.

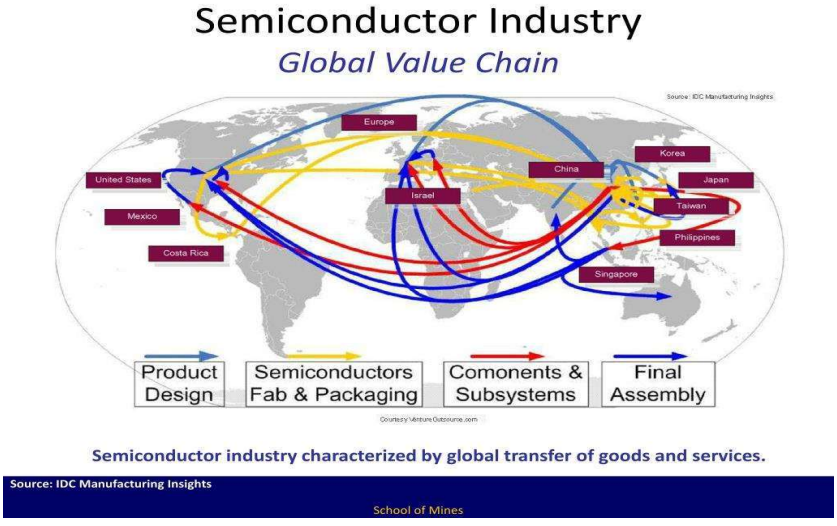

Fig. 6.1.1 Global Semiconductor Value Chain

Global Benefit: This design aligns with global efforts to enhance semiconductor supply chains. R&D in this field could help more regions reduce reliance on dominant producers and increase supply chain resilience by fostering R&D in this field. [34]

Reduction of Carbon Footprint in Semiconductor Production

Impact: With our device design, both reduced leakage current and lower consumption mean a leaner carbon footprint from data centers and consumer electronics.

Global Benefit: Energy consumption reduction in electronic devices aids global climate change mitigation efforts. Our design will lead to efficiency improvements, which will be beneficial for data centers, the world's largest consumers of electricity. [35]

Next-Generation Technologies

Impact: Our design accelerates the development of 5G, AI, and IoT devices, which rely on double-gate NMOS devices with even higher V_{th} and I-V characteristics. This adds to the research around edge computing, AI accelerators, and low-power IoT sensors.

Global Benefit: Next-generation technology providing means for digital inclusion in developing regions is provided in all parts of the globe. IoT and AI technology can open doors to many users, but smaller, cheaper, and more energy-efficient devices will further catalyze the adoption of IoT and AI-enabled systems, which in turn will also contribute to global technological equity. [36]

6.1.4 Summary

Critical challenges in device efficiency, sustainability, and technological progress are faced by our work on the 14 nm double-gate NMOS design. It reduces the cost of production and the competitiveness of semiconductor manufacturers on the market. It is conducive to societally supporting energy-efficient devices, pushing green technology, and growing the talent pool for semiconductor design. Ultimately, the work we do helps drive supply chain resilience across the globe and significantly reduces the carbon footprint of electronics to enable progress in 5G, IoT, and AI technology development. This design is driven by technology, however, the far-reaching impact of our design on our sustainable and inclusive future proves the relevance of our design.

6.2 Environmental and Ethical Considerations

It presents various environmental and ethical considerations during the design and development of a 14 nm double gate NMOS transistor and such considerations relate to sustainability, resource utilization, and the ethical responsibilities of the researchers and engineers. In this section, we outline the most important environmental protection, waste reduction, energy efficiency, and ethical work aspects of this process.

6.2.1 Environmental Considerations

Reduction of Electronic Waste (E-Waste)

Impact: When devices get smaller and use less energy, the lifespan of consumer electronics can be extended. Finally, our NMOS design improves I-V characteristics, reduces power dissipation, and consequently allows longer device lifespans, which in turn helps reduce e-waste generation.

Environmental Benefit: This approach helps reduce the number of discarded devices, or more accurately, e-waste. This is a circular economy principle: electronic components are reused and recycled rather than just binned. [25]

Energy Efficiency Carbon Emission Reduction

Impact: Our NMOS design with an improved threshold voltage (V_{th}) and I-V characteristics especially reduces power consumption and is thus useful to electronic devices like smartphones, laptops, or data centers. Energy consumption is reduced and our design allows a shift to low-carbon electronics.

Environmental Benefit: Low energy usage is needed to reduce carbon emissions. The consumption of this data center power will leverage more power-efficient devices, and all of this has serious implications for global climate change mitigation. [37]

Use of Eco-Friendly Materials

Impact: The barrier, interface, and dielectric layers are made of a $Si_3N_4/ZrO_2/HfO_2$ materials combination. The dielectric constant of the materials used in these is high enough that the layers can be thinner, reducing the number of materials needed and limiting the amount of resource extraction needed.

Environmental Benefit: Reduction of material layer thickness enables reduced resource consumption, reflecting a slight positive impact on resource efficiency. Additionally, high-K dielectrics (such as HfO_2) do not cause more damage to the environment than older materials, like current silicon dioxide (SiO_2), which require a higher temperature of oxidation to do so. [31]

Minimization of Hazards Chemicals and Emissions

Impact: Advanced fabrication techniques create dielectric layers of Si_3N_4, ZrO_2, and HfO_2, but these processes often result in toxic byproducts like volatile organic compounds (VOCs) and hazardous waste. But our goal is to eliminate these toxic materials.

Environmental Benefit: We avoid the exposure of fabrication workers to hazardous chemicals by reducing the elapsed times, minimizing the material layer thickness, and using high-K dielectrics. Furthermore, reduced material requirements reduce waste disposal's environmental impact. [38]

6.2.2 Ethical Considerations

Ethical Responsibility in Sustainable Design

Impact: We point to this imperative for researchers and engineers to design energy-efficient, low-power devices that help reduce energy usage. By planning for sustainability in our devices, we have established good engineering practices that care for future generations.

Ethical Responsibility: The development of energy-efficient transistors reflects the ethical sustainable design principles established in Bangladesh's E-Waste Management Guidelines and Bangladesh Climate Change Strategy and Action Plan (BCCSAP). Once a device follows these policies, we promote lower power consumption of devices, which can help save the environment. It adds to its already agreed compliance with the Asia-Pacific Research Integrity Network (APRIN) and the call by APRIN for the sustainable, transparent development of research and technology.

This study is consistent with the national and regional efforts of sustainability work and in line with the Republic of Bangladesh’s commitment to the Basel Convention on the

Control of Hazardous Wastes and to the Extended Producer Responsibility (EPR) Framework for managing e-waste. The motivation for these initiatives is the desire for semiconductor industry development in a sustainable way, while minimizing environmental degradation, caused by electronic devices. [39]

Research Transparency and Accountability

Impact: Transparency is necessary for conducting ethical research on this project in terms of the methods, materials, and processes employed. Following research integrity principles, we have stuck to the accuracy, verifiability, and reproducibility of our results, our findings, as well as our simulation data and analysis.

Ethical Responsibility: In our study, we make our data collection, simulation results, and interpretations transparent. The ethical research principle requires us to avoid misrepresenting or manipulating the data to draw false conclusions. Open and honest reporting follows because it supports the integrity of scientific knowledge. [40]

Ethical Use of Simulation Software (Silvaco TCAD)

Impact: Using Silvaco TCAD as an example, a licensing agreement and usage rights must be adhered to. These guidelines include adherence to intellectual property (IP) and a software development team.

Ethical Responsibility: All the works are property of Silvaco, so as our ethical commitment, we have complied with Silvaco TCAD licensing requirements and properly cited the software in our research. So, if there was no permission nor compensation, the software would be used in violation of IP laws and academic research would be negatively affected. [41]

Sustainable Development of Advanced Materials

Impact: Si_3N_4, ZrO_2, and HfO_2 materials are becoming more ethically sourced as a concern around the rare earth elements, which are used in semiconductors and are mined in factories used by people working in labor conditions and at the expense of the environment.

Ethical Responsibility: In our design, we try to use fewer rare-earth-based materials and thereby avoid ethical dilemmas such as child labor and forced and environmental

harm. Responsible semiconductor production is fundamentally concerned with ethical material sourcing. [42]

6.2.3 Summary

Our 14 nm double-gate NMOS has many facets for environmental and ethical considerations. On the environmental side, our work contributes to energy efficiency, waste reduction, and using environmentally friendly materials where available. On the ethical side, it helps transparency, sustainability, and compliance with material sourcing standards and licensing standards. Our contribution to global sustainable semiconductor production includes prioritizing resource conservation, reducing e-waste, and responsible research. We also meet ethical guidelines concerning this project by creating credible, reproducible, and beneficial outcomes for this project.

6.3 Utilization of Existing Standards and Guidelines

Parallel fabrication of our 14 nm double gate NMOS transistor has been completed according to the industry standards and guidelines for compatibility, reliability, and ethical research practices. Abiding by these standards assimilates a device better with existing semiconductor technologies and thus enhances design quality and promotes sustainable development. In this section, we list the most important standards and guidelines that we have adhered to in our project.

6.3.1 Semiconductor Design and Manufacturing Standards

ITRS Guidelines for the Year 2009

Utilization: The ITRS is a comprehensive roadmap for semiconductor development, guiding transistor designs, scaling, and performance. The 14 nm double-gate NMOS we've used in this project conforms with ITRS specifications in miniaturization, energy consumption, and use of materials. Using metal gates (TaN) and high-k dielectrics (HfO_2) aligns with ITRS guidelines for low leakage current and easy device characteristics.

Impact: The adherence to the set ITRS standards guarantees that our proposed design competes effectively with the existing semiconductor technologies worldwide and

leaves room for device scaling and power reduction as a factor of industry concern and priority. [43]

IEEE Standards for use by individuals within its organization and the public in related fields.

Utilization: IEEE has set up some fundamental standards for designing, simulating, and testing semiconductor devices. We have followed IEEE Standard 1801 for low power and IEEE 1481 for timing evaluation in integrated circuits. The quality of our simulations, the validity of our data, and the quality of triggering our simulations all greatly depend upon these standards.

Impact: Ultimately, our design meets the timing analysis, power and supply noise, and V_{th} objectives satisfying IEEE standards and therefore contributes to the academic as well as industrial community. [44]

Cleanroom Processes and Standard of Material Quality According to SEMI

Utilization: The Semiconductor Equipment and Materials International (SEMI) organization sets up international guidelines regarding the quality of material, process cleanliness, and contamination of microelectronics fabrication. Hence our layout complies with SEMI S2 regulations on workplace safety and SEMI E10 on equipment reliability and maintainability. Experiments follow the usage of high k dielectrics (HfO_2) and barrier layers (Si_3N_4) under SEMI rules for material cleanliness, thickness control, and accurate deposition.

Impact: SEMl standards are followed for our material deposition processes to deviate minimal defects, high accuracy, and environmental friendliness — to minimize risk in transistor design. [45]

6.3.2 Simulation and Modeling Standards

These guidelines defined in the section below outline the use of Silvaco TCAD tools in the simulation of Analog/Mixed-Signal (AMS) designs:

Utilization: Our simulation process conforms to the general procedures outlined by Silvaco on 2D device modeling. Proper meshing and setting of boundary conditions

and selection of the appropriate physical models of mobility, recombination, and tunneling enable accurate modeling of the 14 nm double-gate NMOS.

Effect: Following the Silvaco TCAD rules makes it easier to repeat our simulations and gives more faith to the analysis of the threshold voltage (V_{th}) and I-V (I_d-V_d). In addition, it gives useful guidelines about how to license software correctly and how to protect property rights. [46]

ISO 9001: Quality Management Systems

Utilization: So, the product development and manufacturing processes are organized according to standards to be specified in ISO 9001. In this work, to keep up international standards, we have embraced ISO 9001 standards, especially on quality matters to ensure quality outcomes on the NMOS device; starting from the design, testing, and analysis stages.

Impact: The work following the guidance of the ISO 9001 from scratch makes our operation more easily reproducible, traceable, and transparent. It fosters the sustainability of the best design practices for continuous enhancement of the quality of our device design. [47]

6.3.3 Ethical and Sustainability Guidelines

Sustainability and Impact Guidelines for Bangladesh

This approach fits Bangladesh's commitment to global sustainability efforts according to the bilateral and multilateral treaties and agreements. For instance, Bangladesh has signed the Paris Climate Change Agreement and other environmental protocols to acquire the maximum from its environmental resources, lowering man's energy consumption and judiciously disposing of electronics. Using high-k dielectrics (HfO_2) along with low thermal budget processes and advanced semantic memory technologies such as RRAM, this study reduces the power consumption of NMOS in the semiconductor design to support Bangladesh's Climate Change Strategy and Action Plan (BCCSAP). This study also aligns with the Bangladesh Environment Conservation Act 1995 by reducing e-waste and promoting eco-friendly technology.

These national and international agreements require compliance, which means responsible engineering practices that have a concern for sustainable development and environmental conservation. This study further aids the environmentally friendly design of semiconductors in the BD electronics industry as Bangladesh grows. The Bangladesh Renewable Energy Policy aims to reduce dependence on non-renewable energy sources by promoting energy-efficient devices. These technologies reduce the environmental footprint of these technologies, thereby protecting the local ecosystem from mission stress and resource depletion as well as pollution and enhancing the process of sustainable economic development and technological innovation in Bangladesh.

General Principles for Ethical Conduct in Research Integrity: Asia and IEEE Codes of Ethics Guidelines

Utilization: Both the IEEE Code of Ethics and the Asia-Pacific Research Integrity Network (APRIN) guidelines for academic research were used to apply ethical consideration principles to the application. These frameworks govern the ethical use of proprietary software, the appropriate exposition of data generated as part of simulations, and proper credit to supporters in academic publications. These standards adhere to help in resource-convenient use and avoid intellectual property violation, particularly software such as Silvaco TCAD and another research tool commonly applied in Asia.

Impact: Such ethics for applying to the research process are sufficient for honesty, transparency, and fairness. It also prevents unfair uses of expensive software (falsification, fabrication, data fabrication, and data manipulation or plagiarism) and it prevents unethical practices. This also increases trust in the research outcomes and hence in the credibility of the field in Asia. They protect against legal and ethical disputes and ensure integrity and cooperation are rife over the region. [48]

Environment Management Act on the Restrictions of Use of Hazardous Substances (RoHS) and the Waste Electrical and Electronic Equipment (WEEE)

Utilization: Restriction of the Use of Certain Hazardous Substances in Electrical and Electronics Equipment (RoHS) is used by us in our design, which is a map of the legal

requirements of restriction of the use of lead, mercury, cadmium, hexamine, and other substances. From a transistor design point of view, our scheme applies to the Waste Electrical and Electronic Equipment (WEEE) directive aimed at ensuring sustainability in the recycling and disposal of semiconductor devices.

Impact: With RoHS and WEEE-compliant designs, we take environmentally friendly approaches to semiconductor manufacturing. I also have eliminated the use of some hazardous materials and the design provides the ability to recycle and dispose of electronics in line with the circular economy model.3. [49]

6.4 Summary

The codes followed in our 14 nm double-gate NMOS transistor design include the Bangladesh Environment Conservation Act, Bangladesh Environment and Conservation Commission Act (1974), the Asia Pacific Research Integrity Network (APRIN) guidelines, Bangladesh National Science and Technology Policy and other relevant international environmental policies and regulatory mechanisms. They standardize the designed device to be safe, reliable, and environmentally sustainable. With high k dielectric, strict adherence to Bangladesh National Quality Standards (as per ISO 9001 principles) and conformity particularly to Asian regional electronic device standards, precision, efficiency and reusability are possible in device manufacturing. The IEEE Code of Ethics and the Asia Pacific Research Integrity Network govern the proper application and citation of software concerning ethical software use. These frameworks support accountability and transparency and the usage of proprietary software such as Silvaco TCAD.

Additionally, this work benefits from adherence to the EPR (Extended Producer Responsibility) principles included under the Bangladesh E-Waste Management Guidelines that emphasize sustainable practices of responsible manufacture, recycling, and waste management. That also fits better with wider efforts worldwide including the Basel Convention that Bangladesh has signed up to curb the negative environmental impact of hazardous waste from the semiconductor industry.

By enforcing these ethical and sustainability principles, this research helps to develop environmentally sustainable and energy-efficient semiconductor technologies in Bangladesh and the Asia Pacific region.

CHAPTER 7
CONCLUSIONS AND RECOMMENDATIONS

7.1 Summary of Our Findings

In this study, we first examined the 14 nm double gate NMOS transistor with the Silvaco TCAD tool. This device performed much better under Vth control conditions and I-V (I_d-V_d) characteristics. By depositing a 0.1nm Si_3N_4 barrier layer, a 0.1nm ZrO_2 interface, and a 0.1nm HfO_2 dielectric, they constructed a multi-layered sandwich structure with improved gate control, reduced SCEs and improved electrostatic integrity. This multiple-layer gate stack with a TaN gate electrode with a work function of 4.3 eV and an aluminum source/drain with a work function of 4.1 eV improves energy band alignment, thus increasing current drive and reducing leakage current.

We found that the leakage current level was significantly reduced. In contrast, the on-state current, as characterized by subthreshold swing, also improved from studies that involved using typical double-gate NMOS configurations. The selected V_{th}=0.14510v is more stable. Further, the proposed design strategy ensures power saving, bringing the device within various contenders for low-power, next-generation transistor applications.

Here, the methodological advancement of the simulation methods and compliance with international standards have helped to overcome some of the shortcomings of existing designs. We demonstrate the possibility of such high-performance, low-power double-gate NMOS transistors for modern semiconductor equipment and systems. We believe that our work provides valuable findings for the transistor scaling topic and is a targeted advancement along the development of semiconductor devices.

7.2 New Skills and Insights Gained Through Our Work

While researching and developing a 14 nm double gate NMOS transistor using Silvaco TCAD, the authors have increasingly sharpened their technical skills, analytical abilities, and research findings to become engineers and researchers. These new competencies have helped improve other broad domains of semiconductor design,

simulation, and optimization techniques. Below are some of the key skills and insights we gained during this project:

Advanced Semiconductor Device Design

Skill Acquired: From the literature we were able to gain a powerful insight into how double-gate MOSFETs are designed, including aspects such as gate control, short-channel effects, and leakage currents. We needed extensive knowledge in material science and thin film deposition and had to integrate a multi-layer dielectric to create the 'sandwich' structure that separated the control gate.

Insight Gained: We deduced how one could alter the device's materials science and the transistor's electrical characteristics. Higher control of the barrier, interface, and dielectric layers led to better electrostatic control, enhancing the threshold voltage (V_{th}) and transfer (I_d-V_d) characteristics.

Proficiency in Silvaco TCAD Simulation

Skill Acquired: There has been progress in our ability to use Silvaco TCAD to simulate a semiconductor device. We were able to gain full control of how to demarcate device geometry, boundary conditions, and pertinent physical models for carrier mobility, recombination, and tunneling.

Insight Gained: We also used the meshing and calibration of the physical models and an accurate selection of parameters to improve the reliability of our results. The understanding and experience gathered in this study will be useful in future designs via simulations, particularly for new nanoscale devices.

Data Analysis and Performance Evaluation

Skill Acquired: This provided us with experience extracting threshold voltage (V_{th}), subthreshold swing, leakage current, and I-V (I_d-V_d) characteristics. We were able to learn what elements and measures to track and determine how certain material options and structural modifications affect device performance.

This study revealed several inconsistencies, indicating that even minor variations in the thickness of the barrier, interface, and dielectric layers can significantly impact the device's performance. We gained knowledge on how to measure and evaluate these

changes within the industry. This insight brought out the fact that nanoscale device fabrication required the highest level of precision engineering.

Application of Industry Standards and Guidelines

We gained a deeper understanding of the ITRS, the IEEE design guidelines, and ISO 9001 in the field of quality assurance. Adopting these standards in the current work raised our work's rigor and reliability by improving the findings' internal validity.

Insight Gained: This made us appreciate the significance of following design compatibility, reproducing work, and the sustainability of the designs we do. We have gathered more information about material quality SEMI guidelines and environmental RoHS/WEEE standards for manufacturing sustainable semiconductors.

Research and Literature Review Skills

Skill Acquired: We enhanced our skills in performing systematic literature reviews, evaluating existing research, and recognizing gaps in the double-gate MOSFET structures. We enhanced productivity by analyzing academic papers and industry patents while comparing approaches taken in the different publications.

Insight Gained: As we conducted the literature review for this research proposal, we operationalized the concept of identifying gaps in the existing literature. That is why there have been considerations to create a ‘sandwich’ gate dielectric structure, which was found to be a special and practical concept in enhancing the transistor’s performance.

Problem-Solving and Critical Thinking

Skill Acquired: We experienced and solved several issues, such as aspects of the divergence during TCAD simulation, problems with the boundary conditions, and concerns over the parameters. All these experiences benefitted us in the improvement of our problem-solving and debugging skills.

Insight Gained: We found out that the use of simulation tools such as Silvaco-TCAD requires patience, trying, and proper thinking. Every issue was solved with a step-by-step procedure and the problem was trying to be isolated. It heightened my skills in

identifying system problems and resolving them, especially in multitiered software systems.

Research Documentation and Technical Writing

Acquired Skills: All of these have contributed to the development of technical writing and research documentation production, particularly in preparing detailed reports, technical papers, and our final thesis. We have expanded our capabilities to structure, organize, and present research data in a comprehensible, coherent, and professional manner.

We gained insight into the importance of documentation in disseminating research findings. Documentation of the steps, assumptions, and limitations of our simulation work helped provide evidence, as well as blame the work. This makes us better placed for future jobs that have accurate technical writing tasks.

Collaboration and Project Management

Skill Acquired: We fashioned our teamwork and project handling skills, such as the division of work and assignments, and tracking of project achievements and project schedules, respectively. Key factors in accomplishing various tasks on schedule were coordinating mechanisms and communication.

Insight Gained: Big projects must be done with real teamwork and assignment distribution. Managing a project taught me a few things: identifying, evaluating, and selecting key deliverables; planning the resources needed to do each deliverable and preparing for how far a project is along.

7.2.1 Conclusion

The 14 nm double-gate NMOS transistor learning enabled me to develop technical, analytical, and research skills. We were able to master handling Silvaco TCAD layout or editing based on screenshots, we were able to familiarize ourselves with the concepts used in semiconductor design and we improved in terms of identifying and comparing performance based on certain parameters such as V_{th} and I_d-V_d. Moreover, we have learned about requirements concerning industry standards, sustainable design, and ethical practice, as well as enhanced our understanding of the expectations of

semiconductor engineers. These skills and knowledge have prepared us to advance to higher education, participate in industry-relevant research and development, or contribute to the creation of new semiconductor designs.

7.3 Recommendations for Future Research and Development

Based on our investigation of the 14 nm double-gate NMOS using Silvaco TCAD, several recommendations for future R&D are identified, based on the findings and insights gained. We address the limitations in the double gate MOSFET performance and scalability, explore new design prospects, and improve the performance and scalability through these recommendations. Our key recommendations are as follows:

Alternative High-k Dielectric Materials

Reasoning: Even though our "sandwich" structure with Si_3N_4, ZrO_2, and HfO_2 does a better job of controlling threshold voltage (V_{th}) and leakage current, other high-k dielectric materials may be better.

Recommendation: Future research should explore alternative materials like La_2O_3, TiO_2 or the rare earth oxides, which could have dielectric constants higher than that of the TaN, stable at higher temperatures, or are compatible with the TaN electrode are to be explored. Thirdly, we should investigate whether the material can remain stable at high temperatures to establish a process-compatible material.

Potential Effects: Making ultra-small devices (less than 10 nm) and improving electrostatic control even more means finding better dielectrics to reduce leakage current.

Optimization of Layer Thickness and Material Composition

Rationale: In our study, we fix the thickness of the Si_3N_4, ZrO_2, and HfO_2 layers to 0.1 nm each. However different thicknesses of these layers relative to each other could result in better tradeoffs between leakage current, $V_{th,}$ and subthreshold swing.

Recommendation: Future work should focus on specific electrical characteristics of the “sandwich” device while varying the thickness of each layer therein. It could be based

on the design of experiments (DOE) and machine learning (ML) to find the optimal layer combination.

Potential Impact: For these low-power, high-performance devices this optimization can lead to more efficient designs that have better control over sub-threshold leakage and overall power consumption.

Investigation of Alternative Gate Electrode Materials

Rationale: We worked with a TaN gate electrode with a work function of 4.3 eV. However, the V_{th} improvement seen with this material was offset by better compatibility or better carrier distribution control for other metals.

Recommendation: Other materials than GaN such as TiN, WN, or dual metal gate stacks and R&D of future materials should be looked into, which may hold better energy level alignment. As a result, work function engineering should optimize V_{th} to meet the functional requirements of specific applications.

Potential Effects: Changing the gate electrode's work function to tune V_{th} may give more V_{th} tuning options, making the technology more useful for a wider range of devices, including low-power ones and fast processors.

Analysis of Temperature Dependence and Reliability Testing

Rationale: Our study works mainly under standard operating conditions and electrical characteristics. Real-world semiconductor devices, however, suffer from variations in temperature, stress, and aging over time.

Recommendation: Thus, future research should study the thermal stability of the "sandwich" gate structure to capture its resistance to high-temperature processing or long-term reliability. TDDB and BTI studies are recommended.

Potential Impact: Reliability testing can be enhanced to improve device stability under multiple operating conditions, improving the commercial viability of this transistor design for next-generation electronics.

Exploration of Quantum and Tunneling Effects

Rationale: Effective carrier mobility and leakage current are strongly influenced by device dimensions and quantum confinement, as well as tunneling effects in the channel, since the 14 nm node and beyond.

In addition, quantum effects should also be investigated on the channel, in the vicinity of the source and drain junctions. Carrier flow could be better understood using quantum transport models and the non-equilibrium Green's function approach.

Potential Impact: This will help us to address quantum effects and help devices at even smaller nodes (10 nm, 7 nm, and 5 nm) and to control leakage more precisely, thus ensuring Moore's Law.

Development of Power-Efficient and Low-Leakage Variants

Rationale: However, future mobile and wearable devices will demand even more power consumption and our design will achieve better I-V (I_d-V_d) characteristics.

Recommendation: Future R&D should aim for ultra-low-power designs by lowering the subthreshold switch and leakage current. The thresholds might be adaptive techniques and perhaps the biases as well.

Potential Impact: Incompatible with energy-efficient applications such as wearable devices, IoT sensors, and embedded electronics, ultra-low power devices are targeted. The findings could help make it easier to build more efficient semiconductor devices that operate longer on the battery.

Incorporation of Sustainable and Environmentally Friendly Materials

Rationale: The semiconductor industry has started greening and RoHS, WEEE, and other environmental standards compliance.

Recommendation: Future development should focus on non-toxic, recyclable materials for electrodes, interconnects, and gate stacks. Materials with less environmental impact are a concern of first order within the world's goal for global sustainability.

Rationale: The semiconductor industry is in the direction of green practices and RoHS, WEEE, and compliance with other environmental standards.

Recommendation: The use of nontoxic, recyclable materials for electrodes, interconnects and gate stacks should be concentrated in future development as well. To achieve global sustainability goals, rates of use of environment-degrading materials must be reduced.

Integration of 3D Architectures and Beyond CMOS Technologies

Rationale: Green is the order of the day and the semiconductor industry is striving for compliance with RoHS, WEEE, and other environmental compliance standards.

Recommendation: In the future, electrode, interconnect and gate stack materials should use nontoxic, recyclable materials. Global sustainability prioritizes materials with less environmental impact.

Integration of Machine Learning in Device Optimization

Rationale: Optimization of device parameters is tedious and time-consuming. Machine learning (ML) can accelerate this process.

Recommendation: We recommend that researchers further investigate the automation of the 'sandwich' gate structure via ML algorithms. The solution is to train ML models on large datasets from TCAD simulations to predict the best combinations in opt fluidic materials, thicknesses, and electrical properties.

Potential Impact: ML-driven optimization could lead to enormous development time reduction as well as rapid determination of optimal configurations. The approach could give rise to "smart design" flows for future transistors.

Alternative Channel Materials Investigations

Rationale: However, since the standard channel medium of NMOS is silicon, there are other materials, such as germanium (Ge), as well as 2D materials like MoS_2 and graphene, that can provide higher mobility.

Recommendation: Further research is needed to explore how the 'sandwich' gate design performs with Ge or 2D materials as the channel. For flexible and transparent electronics, we could integrate with 2D materials.

Potential Impact: High-mobility channel material may be used in conjunction with high-mobility materials to create extended channel transistors with improved performance, particularly where ultra-high speed or flexible electronics are desired.

7.3.1 Conclusion

The remaining problems in the development of double-gate NMOS technology, especially choosing the right material, have to do with making the device architecture and simulation methods even better. Therefore, our recommendations for future research and development focus on the exploration of alternative materials, multi-objective optimization, and sustainable manufacturing. By tackling leakage, power consumption, and environmental impact, we can manufacture next-generation semiconductor devices with green, highly efficient, and reliable transistors. Based on our results, we expect future advances in low-power electronics, ultra-dense chip integration, and sustainable manufacturing.

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APPENDIX A
TURNITIN REPORT

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APPENDIX B
PROGRAM CODE

```
go atlas

# Set mesh spacing multiplier
mesh space.multi=1.0

# Define x-direction mesh points with specific spacings for refined grid
x.mesh loc=0.000  spac=0.01
x.mesh loc=0.009  spac=0.01
x.mesh loc=0.010  spac=0.0001
x.mesh loc=0.011  spac=0.01
x.mesh loc=0.012  spac=0.01
x.mesh loc=0.013  spac=0.01
x.mesh loc=0.014  spac=0.01
x.mesh loc=0.0145 spac=0.0001
x.mesh loc=0.015  spac=0.0001
x.mesh loc=0.016  spac=0.0001
x.mesh loc=0.0165 spac=0.0001
x.mesh loc=0.017  spac=0.01
x.mesh loc=0.018  spac=0.01
x.mesh loc=0.019  spac=0.01
x.mesh loc=0.020  spac=0.01
x.mesh loc=0.021  spac=0.01
x.mesh loc=0.022  spac=0.01
x.mesh loc=0.023  spac=0.01
x.mesh loc=0.024  spac=0.01
x.mesh loc=0.025  spac=0.01
x.mesh loc=0.026  spac=0.01
x.mesh loc=0.027  spac=0.01
x.mesh loc=0.028  spac=0.01
x.mesh loc=0.029  spac=0.0001
x.mesh loc=0.030  spac=0.0001
x.mesh loc=0.031  spac=0.01
x.mesh loc=0.032  spac=0.01
x.mesh loc=0.033  spac=0.01
x.mesh loc=0.034  spac=0.01
x.mesh loc=0.035  spac=0.0001
x.mesh loc=0.036  spac=0.01
x.mesh loc=0.045  spac=0.01

# Define y-direction mesh points with adjusted spacings for material boundaries
```

```
y.mesh loc=0.000      spac=0.1
y.mesh loc=0.001      spac=0.1
y.mesh loc=0.002      spac=0.1
y.mesh loc=0.003      spac=0.1
y.mesh loc=0.004      spac=0.01
y.mesh loc=0.005      spac=0.001
y.mesh loc=0.006      spac=0.0001
y.mesh loc=0.007      spac=0.001
y.mesh loc=0.008      spac=0.001
y.mesh loc=0.009      spac=0.01
y.mesh loc=0.010      spac=0.1
y.mesh loc=0.011      spac=0.01
y.mesh loc=0.012      spac=0.001
y.mesh loc=0.013      spac=0.001
y.mesh loc=0.014      spac=0.0001
y.mesh loc=0.015      spac=0.001
y.mesh loc=0.016      spac=0.01
y.mesh loc=0.017      spac=0.1
y.mesh loc=0.018      spac=0.1
y.mesh loc=0.019      spac=0.1
y.mesh loc=0.020      spac=0.1


# Define material regions in the device structure
region num=1  material=          air                  x.min=0
        y.min=0


region num=2  material=          silicon                    x.min=0.01000
        X.max=0.01550            y.min=0.0060 y.max=0.0140
region num=3  material=          silicon              x.min=0.01550
        X.max=0.02950            y.min=0.0060 y.max=0.0140
region num=4  material=          silicon              x.min=0.02950
        X.max=0.03500            y.min=0.0060 y.max=0.0140


region num=5  material=     ZrO2                      x.min=0.01000
        X.max=0.03500            y.min=0.0059 y.max=0.0060
region num=6  material=          HfO2                       x.min=0.01000
        X.max=0.03500            y.min=0.0058 y.max=0.0059
region num=13 material=        Si3N4                        x.min=0.01000
        X.max=0.03500            y.min=0.0057 y.max=0.0058
region num=7  material=          TaN                        x.min=0.01550
        X.max=0.02950            y.min=0.0000 y.max=0.0057
region num=8  material=     ZrO2                      x.min=0.01000
X.max=0.03500            y.min=0.0140   y.max=0.0141
```

```
region num=9  material=          HfO2                    x.min=0.01000
      X.max=0.03500              y.min=0.0141 y.max=0.0142
region num=14 material=          Si3N4                   x.min=0.01000
      X.max=0.03500              y.min=0.0142 y.max=0.0143
region num=10 material=          TaN                     x.min=0.01550
      X.max=0.02950              y.min=0.0143 y.max=0.0200
region num=11 material=          aluminum                x.min=0.00000
      X.max=0.01000              y.min=0.0033 y.max=0.0167
region num=12 material=          aluminum                x.min=0.03500
      X.max=0.04500              y.min=0.0033 y.max=0.0167
```

```
# Define electrode locations and types
# Top gate electrode
electrode      reg=7        name=gate     material=TaN
# Bottom gate electrode
electrode      reg=10       name=gate1    material=TaN
# Source electrode
electrode      reg=11       name=source   material=aluminum
# Drain electrode
electrode      reg=12       name=drain    material=aluminum
```

```
# Define doping concentrations for different regions
# High n-type doping in source region
doping uniform concentration=1E20 n.type region=2
# P-type doping in channel region
doping uniform concentration=1E14 p.type region=3
# High n-type doping in drain region
doping uniform concentration=1E20 n.type region=4
```

```
# Define contact properties
#workfunction=4.3 for TaN
# Set work function for gate contact
contact name=gate workfun=4.3
# Set work function for bottom gate
contact name=gate1 workfun=4.3 common=gate
# Neutral contact for source
contact name=source workfun=4.1
# Neutral contact for drain
contact name=drain workfun=4.1
```

```
# Activate models for mobility, recombination, and field effects
models conmob srh auger bgn fldmob print CVT

# Set solution method parameters
method newton itlimit=25 maxtrap=4

# Define output quantities for simulation data
output val.band con.band qfn qfp e.field j.electron j.hole j.conduction j.total ex.field
ey.field flowline e.mobility h.mobility qss e.temp h.temp j.disp



# IDVG
solve init
solve vdrain=0.1 outf=vd0.1
solve vdrain=0.2 outf=vd0.2
solve vdrain=1 outf=vd1

# Load each structure and solve for gate voltage sweep
load infile=vd0.1
log outf=vd0.1.log master
solve ac frequency=1e6 name=gate  vgate=0 vstep=0.1 vfinal=1
log off

load infile=vd0.2
log outf=vd0.2.log master
solve ac frequency=1e6 name=gate vgate=0 vstep=0.1 vfinal=1
log off

load infile=vd1
log outf=vd1.log master
solve ac frequency=1e6 name=gate vgate=0 vstep=0.1 vfinal=1
log off



# IDVD
solve init
solve vgate=0.1 outf=v0.1
solve vgate=0.2 outf=v0.2
solve vgate=0.5 outf=v0.5
solve vgate=1 outf=v1

# Load each structure and solve for drain voltage sweep
load infile=v0.1
log outf=v0.1.log master
solve name=drain vdrain=0 vstep=0.1 vfinal=5
```

```
log off

load infile=v0.2
log outf=v0.2.log master
solve name=drain vdrain=0 vstep=0.1 vfinal=1
log off

load infile=v0.5
log outf=v0.5.log master
solve name=drain vdrain=0 vstep=0.1 vfinal=1
log off

load infile=v1
log outf=v1.log master
solve name=drain vdrain=0 vstep=0.1 vfinal=1
log off



# End

extract init inf="vd1.log"
extract name="Vth" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))))
extract name="Ion/Ioff" ((max(abs(i."drain")))/min(abs(i."drain")))
extract name="Ioff" (min(abs(i."drain")))
extract name="Ion" (max(abs(i."drain")))
extract name="Ileak" (min(abs(i."drain")))


# Save final structure file
save outf=TaN.str

# plot data
tonyplot TaN.str
tonyplot -overlay      vd0.1.log      vd0.2.log                    vd1.log
tonyplot -overlay      v0.1.log       v0.2.log       v0.5.log      v1.log



quit
```