FAULT DIAGNOSIS METHODS IN ANALOG AND MIXED SIGNAL CIRCUITS: A REVIEW

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Abstract: Fault identification of analog and mixed signal circuits is very difficult topics for previous few decades. Localization of hard and soft faults in analog circuit is often a troublesome task without a transparent cut methodology. For manufacturing process of Very Large Scale Integration (VLSI) Application Specific Integrated Circuits (ASICs) both fault diagnosis and localization are mandatory. The importance of such analog test has become important due to enhancement of networking and communication sector. This paper gives a brief review on the faults present in analog circuits and different diagnosis methodologies of these faults. Comparison of detection is also demonstrated among some techniques for some of the ITC97 Benchmark circuits.

Keywords: *Simulation after Test (SAT); Simulation before Test (SBT); Built-in Self-Test (BIST); fault; Integrated Circuits testing; tolerance; detectability.*

1. INTRODUCTION

The world is experiencing the revolution of VLSI circuits in the sense that the application and consumption of such circuits are increasing very fast, enhancing the financial growth at a top rate. Although many challenges still exist in analog IC production regarding design aspects, performance analysis of these circuits is still the most critical issue [1]. Now it has become more difficult to determine both the catastrophic and parametric faults as analog circuits show nonlinear characteristics generally [2]. When the system variation and tolerance are negligible while the number of practically accessible nodes is small in number, the fault diagnosis techniques have eventually expanded. Development of fault testing methodologies has eventually established itself as one of the most assiduous task for the researchers all over the world due to its need for perfection for achieving as much correct outcome as possible. There are also some algorithms where optimal test point of analog circuit can be located using Fault Detection and Isolation Information (FDI) Coding [3].

In Section II, a review of different types of faults present in analog circuit is made. Section III describes various diagnosis methods utilized for fault detection, identification and localization. Finally, Section IV concludes with the achievements of this methods and the future improvement goals.

2. EXISTING FAULTS IN ANALOG CIRCUITS

The total mechanism of existing faults has been discussed in this section. Usually a fault model for analog circuit suggests theoretical values that simulate attainable faults existing in ICs [3]. Simulation of faults involves behavioral modeling as well as parametric variation. So fault modeling is an important aspect in fault detection, identification and localization. Some faults are classified in Table I. The parametric variation of the components from nominal value of VLSI ICs can be done to classify the basic faults-

(i) Manufacturing tolerances: This tolerance level depends on manufacturing process and fault level. That is why they are very difficult to find out exactly.

(ii) Soft faults: Soft faults are also known as parametric faults and can be determined by SAT (Simulation after Test). Parametric faults depend on the range of manufacturing tolerance.

(iii) Hard faults: Hard faults which are also known as catastrophic faults significantly depend on the tolerance level of manufacturing ICs. This type of fault can occur due to over ageing of IC component or defect in design. Diagnosis process can be SAT as well as SBT for hard faults.

(iv) Fatal-faults: The fault effect of large deviation ranges from complete malfunction of the circuit. Table II shows the ranges of different faults. However, parametric faults are more difficult because the relation between the parametric deviation and performance degradation is very complicated.

Categories of defects and faults have been shown separately.

TABLE I. CATEGORIES of DEFECTS and FAULTS

Fault (effects)			
Detect Causes	***All performance within specified limits***	***Soft fault (output deviation medium)***	***Catastrophic fault (output deviation large)***
Process parameter within specified limit	A1 (Defect and Fault free)	A2	A3
Process parameter outside specified limit	B1	B2	B3
Shorts and opens	C1	C2	C3

3. MODERN METHODS OF FAULT DIAGNOSIS

Two basic localization techniques are described in this section.

A. Simulation After Test (SAT) Methods

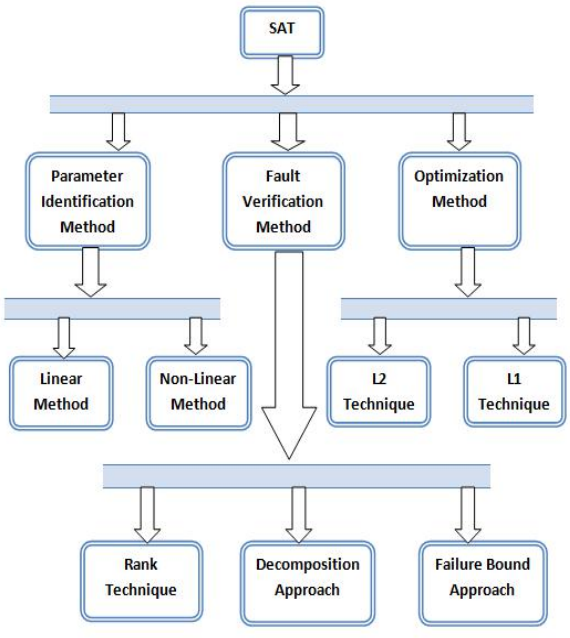

Fig. 1. Classification of SAT

- Parameter Identification Method: Depending on the linear and non- linear equations of analog circuit testing parameters, parameter localization process can be classified in two categories.
- Determination of Fault Methods: Three different processes can be used including rank, decomposition and failure bound approach.

Rank Techniques: By applying rank technique, rank of a certain matrix is used to identify the faults. An impedance matrix is used, in which each column corresponds to a fault.

Decomposition Approach: In this method the network is decomposed into sub-networks using the measurement nodes. Under certain testing conditions, the logical analysis is performed to identify the faulty sub-networks. Improved Methods are also proposed to reduce error in the decomposition approach.

Failure Bound Approach: This method uses a bound on the number of faulty elements. Faulty parameters are identified under the assumption of limited faults and limited test point availability. A theoretical characterization of the failure bound technique has been developed [5]. A method which is based on nodal analysis, to locate sub-networks containing all faults has been presented also.

Optimization Methods: There are two methods- L2 approximation techniques for error analysis of system and L1 approximation technique to isolate the most likely faults.

B. Simulation Before Test (SBT) Methods

Research methods available in SBT approach are mainly categorized in two ways [6]-

Fault Dictionary methods and Statistical Methods.

Fault Dictionary method: Applicable for both linear and non-linear characteristics of analog circuits. Table II describes the faults range for corresponding faults.

TABLE II. RANGES of DIFFERENT FAULTS

Fault Name	Ranges (in percent)
Manufacturing tolerances	-1 to +1
Hard faults	-50 to +100
Soft faults	-10 to +10
Fatal faults	Open or short circuit

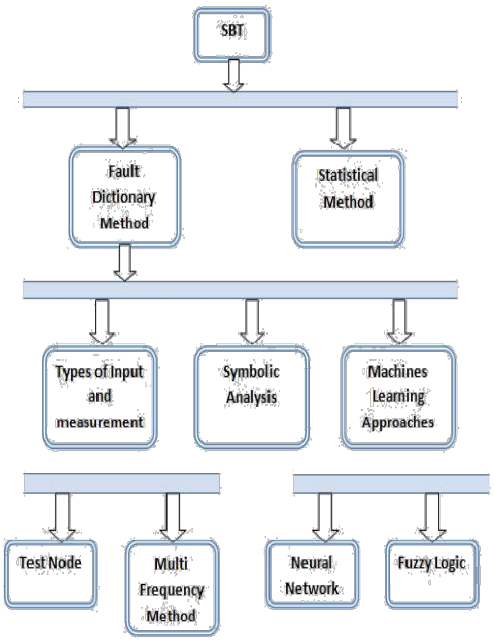

Fig. 2. Classification of SBT

Fault Dictionary method: This method is based of the manufacturing process and size. These are: (i) Input/ Output analysis methods. (ii) Machine Learning and Neural Networks (iii) Analysis of Symbol.
Figure 1 and Figure 2 demonstrates simple block diagram of SAT and SBT techniques.

TABLE III. COMPARISON of SOME IMPORTANT ANALOG FAULT DIAGNOSIS TECHNIQUES

Method	Test Nodes	Test Frequencies	Faults	Networks
Fault Dictionary	Limited	Minimal	Single	Linear/ non-linear
Linear Parameter Identification	Almost all nodes	No	Multiple	Linear/ non-linear
Failure Bounds	Limited	No	Multiple	Mostly linear
Network Decomposition	Limited	No	Multiple	Linear/ Non-linear
Neural Networks	Limited	Minimal	Mostly single	Linear/ Non-linear
Symbolic analysis	Maximum Nodes	Minimal	Multiple	Linear/ Non-linear

(i) Input/ Output Analysis Methods: (a) Test Nodes: There are a number of nodes for testing circuits in these methods depending on Boolean algebra. These nodes will separate the part of ICs for testing purpose. (b) Multi Frequency Methods: Frequency response is used to classify faults in an analog circuit and the peak frequency and amplitude is used to classify faulty and fault free circuit.

(ii)Machine Learning Approaches: Basic two types:

Neural Networks and Fuzzy Logics: In general Neural Network method uses a systematic procedure which reduces the number of simulations required, without reducing the number of faults.

(iii)Symbolic Analysis: In case of any analog circuits, if the parameter differ a lot with respect to the original or ideal value, symbolic analysis is preferred. This process can be applied with the knowledge of numerical analysis for testing.

C. By Using Supply Current Measurements

This method computes the supply current of analog and mixed circuits and detects or diagnoses faults based on RMS (root mean square) and spectrum calculations of the supply current and corresponding fault dictionary. Full hard fault coverage has been achieved by this method.

D. Fault Diagnosis Using Simple Time Domain Analysis

For an SBT process the golden circuit is simulated with predetermined test stimuli at all or required design corners and the CUT is simulated with those test stimuli at those corners and simulation results of two sets of data are compared. Obtained RMS value is compared with a predefined value and the decision is made whether the CUT is faulty or non-faulty. Simple time domain analysis shows poor result than other advanced techniques. It is hard to diagnosis the characteristics of the fault more precisely with this technique.

E. Use of DFT in Fault Diagnosis

The main advantage in using DFT is that it can resolve the output waveform into all the frequency components that shows the differences between faulty and golden circuit waveform even when the differences between this waveform are small in time domain [7]. The coefficients of Fourier transform of

golden circuit and CUT is calculated. The difference between the coefficients is calculated using normalized rms error directly from the magnitude of the coefficients of the signals. The error can also be calculated from the phase spectrum of the coefficients based on the phase shift due to the fault or even from energy spectrum obtained using magnitude spectrum. Studies done over the years in search of efficient techniques of fault detection using Fourier transform of obtained signals of output voltage.

F. Wavelet Analysis

Wavelet transform is developed to overcome the limitations that Fourier Transform has. This process has shown prospective advantages in fault diagnosis [8-9]. In diagnosis of faults, the CUT is excited using specified test stimuli and the response is transformed into equivalent wavelet transform using a wavelet basis. The CUT response is decomposed into corresponding approximate and detail coefficients for each set of sampled data. This obtained set of coefficient values is then compared with similar type of set of coefficient obtained by wavelet transform of the response of golden circuit. The differences from comparison are then used for fault identification using proper detection method.

G. Use of Frequency Response in Fault Detection

Frequency response of a circuit can be used to determine if any atypical incident has occurred within the circuit. The frequency response of a fault free golden circuit is obtained beforehand. Test signals of varying frequencies are applied to the circuit under test to obtain its frequency response [10].

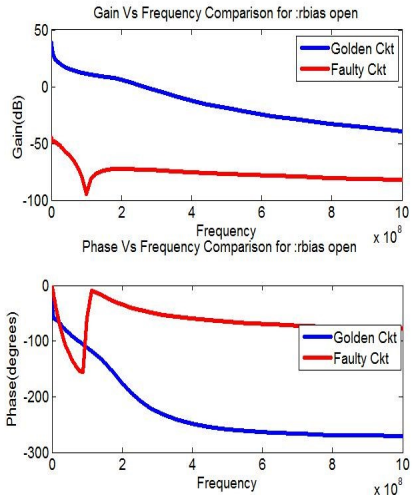

Fig. 3. Waveform of golden and faulty circuit

H. Fault Simulation with Sub-circuits

Under this method, the circuit under test is divided into several sub circuits and then simulation process in done. From the analysis it can be shown that fault coverage from DC test is determined more accurately [11].

The comparison of these two frequency responses is used to diagnosis the fault. A significant deviation in the frequency response parameter values clearly suggests the occurrence of a fault inside the circuit. Figure 3 represent waveforms of golden and faulty circuits showing frequency response against gain and phase of output voltage [12].

Here Table IV demonstrates the Comparison of Fault Detection Using Gain Vs Frequency among the Benchmark Circuits. From the analysis it can be said that the lowest number of total possible faults can occur in Single Stage Amplifier and highest number of fault can occur in Leapfrog filter. 100% gain is detectable in Opamp1 where as in Single Stage amplifier, the gain detect ability is almost half than Opamp circuit.

Again TABLE V. explains the Comparison of Fault Detect ability Using Vector analysis using gain and phase.

TABLE IV. Comparison of Fault Detection Using Gain Vs Frequency among the Benchmark Circuits

Name	Source	Total no. of possible faults	detectable faults by gain	Gain detectability (Percent)
Opamp1	ITC' 97 [1]	28	28	100
Opamp2	ITC' 97 [1]	20	20	80
Comparator	SFA [5][6]	26	21	80.7692
CTSV filter	ITC' 97 [1]	84	67	79.7619
Elliptical Amplifier	SFA [5][6]	104	77	74.0384
Leapfrog filter	ITC' 97 [1]	154	116	75.3246
Low pass filter	Lucent Tech	28	24	85.7142
Digital to Analog Converter	ITC' 97 [1]	104	91	87.5
Single Stage Amplifier	SFA [5][6]	18	9	50
Differential Amplifier	SFA [5][6]	42	35	83.333

TABLE V. Comparison of Fault Detectability Using Vector Technique among Some Benchmark Circuits

Circuit Under Test	Gain detectability (percent)	Phase detectability (percent)	Vector detectability (percent)
CTSV Filter	84.5	97.6	89.3
Leapfrog Filter	75.3	75.3	75.3
Elliptical Amplifier	82.7	81.7	82.7
Single Stage Amplifier	50	38.8889	50
Differential Amplifier	83.3333	88.095	85.7143

Major problem for analog circuit includes internal nodes and fault masking. By applying tolerance maximization process these obstacle can be solved for better result.

CONCLUSION

In this paper, different fault diagnosis has been analyzed on various bases. The study involved time domain analysis, frequency domain analysis, wavelet analysis as well as a detail analysis on frequency response applying Simulation before Test (SBT) approach. Comparison of results from different methods pro-vided us with a suggestion of using wavelet analysis for fault detection. We have also discussed Vector technique that uses the combination of gain and phase variation of output voltage with frequency. It is observed that vector technique shows better performance in fault diagnosis than other certain methods. Furthermore, we have compared percentage of detections of the Benchmark circuits in Table IV. The methods used in fault diagnosis of ICs is developing now a days offering more accurate results and help keeping pace with the increment of the electronic production.

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