# ANALYSIS OF ISOLATED DC-DC CONVERTERS WITH REDUCED NUMBER OF POWER SWITCHES 

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DEPERTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING Daffodil International University, NOVEMBER, 2020

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# ANALYSIS OF ISOLATED DC-DC CONVERTERS WITH REDUCED NUMBER OF POWER SWITCHES 

## A THESIS

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Under Supervision of

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#### Abstract

Nowadays there are many kinds of familiar dc-dc topologies are available used in many applications such as earth-moving equipment, heavy trucks, marine vehicles etc. The main problem of this topologies and also conventional one is use more switches that increasing the power losses and decreasing efficiency. To overcome this problem an isolated dc-dc converter with reduced number of power switches are provided. To use this proposed converter which reduce the losses and increase efficiency. The selected simulated and experimental results are presented as well.


## CHAPTER-I: INTRODUCTION

### 1.1 INTRODUCTION

Before the development of power semiconductors and allied technologies, one way to convert the voltage of a DC supply to a higher voltage, for low-power applications, was to convert it to AC by using a vibrator, followed by a step-up transformer and rectifier[1]. For higher power an electric motor was used to drive a generator of the desired voltage sometimes combined into a single "dynamotor" unit, a motor and generator combined into one unit, with one winding driving the motor and the other generating the output voltage. These were relatively inefficiency [2].

### 1.2 POWER PROCESSING

In the beginning, power electronics [3], [4], mainly focused on advancing devices that provide the capability to handle high power levels. Then the focus transitioned to the application of the semiconductor devices with suitable power rating to meet broader requirements of novel products. Recently it was expanded to multidisciplinary technology such as artificial intelligence and neural network [5].


Fig. 1.1 Electric Power Conversion System

In the field of power processing system, efficiency is a vital factor. Considered Pout is the output power and Pin is the input power then efficiency $\eta$ is,
$\eta=\frac{\text { Pout }}{\text { Pin }}$
The power losses is the difference between the input and output power. The power losses is,
Power losses $=$ Pin - Pout

$$
\begin{align*}
& =\frac{\text { Pout }}{\eta}-\text { Pout }  \tag{1.2}\\
& =\operatorname{Pout}\left(\frac{1}{\eta}-1\right) \tag{1.3}
\end{align*}
$$

Therefore,

$$
\begin{equation*}
\frac{\text { Ploss }}{\text { Pout }}=\left(\frac{1}{\eta}-1\right) \tag{1.4}
\end{equation*}
$$

The equation of (1.4) is plotted in MS Excel to generate the graph to depict the ratio of power loss to output power versus the efficiency of the converter.


Fig. 1.2. Power Loss vs. Efficiency curve of converter

The electronic power conversion process can be done one of four types:

1. Alternating current (AC) to direct current(DC)
2. Direct current (DC) to alternating current(DC)
3. Direct current (DC) to direct current(DC)
4. Alternating current (AC) to alternating current(DC)

In this thesis, the dc to dc conversion then were taken into consideration.

### 1.3 DC-DC CONVERTER

In 1940's, the dc-dc converter was proposed and widely used in industrial application, computer hardware circuitry and high power and high voltage related applications. Switching mode dc-dc converters are more efficient then linear converters as the transistors operate as switches and dissipate less power. PWM dc-dc converters are capable of conducting in step-up, step-down mode and can have multiple output voltages whereas linear regulators can operate only as stepdown converters [6]. High step-up converters are especially required in the wide range of applications of energy sources like photo-voltaic panels and fuel cells which have variable input voltage range and low output voltage [7], [8]. High-voltage direct current (HVDC) transmission systems have lower cable loss than high-voltage alternating current (HVAC) transmission systems [9]. HVDC technology is considered as the main element of multi-terminal grid [10].

### 1.4 ISOLATED DC-DC CONVERTER

The isolation refers to the existence of an electrical barrier between the input and output of the DC-DC converter. An isolated DC-DC converter will have a high frequency transformer providing that barrier [a]. An interleaved converter with voltage multiplier was proposed in [11] that has reduced switching loss but this kind of converter lacks proper control system in applications other than electric vehicles. Cascade technique along with inductor coupling was implemented for high step-up operation in [12]. But over these traditional converters, isolated dc-dc converters have many advantages in electrical isolation, high reliability, ease of realizing soft switching control and bidirectional energy
flow [13]. Another important factor is that three-level full bridge converters are able to reduced losses and improved the efficiency with reduced number of switches as compared to the two-level dc-dc converters.

Therefore, in this thesis, full bridge isolated type converter is considered.

## CHAPTER -II <br> BACKGROUND CONFIGURATION

### 2.1 INTRODUCTION

Isolation means the electrical separation between the input and output of a DC-DC converter [14]. An isolated DC-DC converter uses a transformer to eliminate the dc path between its input and output [15]. The isolated DC-DC converter used for medium voltage range [16]. In this type of configuration full bridge circuit used for input and output voltage significantly proportionate. This converter is excellent for storage energy system [17].

### 2.2 SINGLE INPUT SINGLE OUTPUT DC-DC CONVERTER

### 2.2.1 CONVERTER CONFIGURATION

A single input single output dc-dc converter shown in Fig.2.1


Fig. 2.1. Full-bridge Single Input Single Output Dc-Dc Converter
The transformer primary side consists of four switches and secondary sides consist bridge rectifier and LC filter. The LC filter is used for removing distortion. Transformer turns ratio is $1: \mathrm{n}$ from primary to secondary side.
The transfer function of the converter is,

$$
\begin{equation*}
\mathrm{v}_{\text {out }} / \mathrm{v}_{\mathrm{in}}=\mathrm{n} * \mathrm{D} \tag{2.1}
\end{equation*}
$$

where, $\mathrm{n}=$ Secondary turn
D=Duty cycle

### 2.2.2 SWITCHING SIGNALS

The switching signals convert AC voltage in the transformer primary because the transformer never convert DC voltage. The generated voltage is control the duty cycle. The possible four switching state is $2^{4}=16$ shown in Table 2.1.

TABLE-2.1
ALL POSSIBLE STATE OF THE FOUR SWITCHES

| state | Q1 | Q2 | Q3 | Q4 | V $_{\text {pri }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 0 | 0 |
| 4 | 0 | 0 | 1 | 1 | 0 |
| 5 | 0 | 1 | 0 | 0 | 0 |
| 6 | 0 | 1 | 0 | 1 | 0 |
| 7 | 0 | 1 | 1 | 0 | $-\mathrm{V}_{\text {in }}$ |
| 8 | 0 | 1 | 1 | 1 | 0 |
| 9 | 1 | 0 | 0 | 0 | 0 |
| 10 | 1 | 0 | 0 | 1 | $V_{\text {in }}$ |
| 11 | 1 | 0 | 1 | 0 | 0 |
| 12 | 1 | 0 | 1 | 1 | 0 |
| 13 | 1 | 1 | 0 | 0 | 0 |
| 14 | 1 | 1 | 0 | 1 | 0 |
| 15 | 1 | 1 | 1 | 0 | 0 |
| 16 | 1 | 1 | 1 | 1 | 0 |
|  |  |  |  |  |  |

The switching signals of the converter need to be such that it generates an AC. When the primary is open circuited or shorted then primary voltage of transformer is zero. When the S2 and S3 is on then transformer primary is negative voltage and when S1 and S4 is on then transformer primary is positive voltage.so the state number 7 and 10 is produce negative and positive voltage in transformer primary respectively. Also while choosing the zero voltage states it should be such that it makes the Boolean expression less complicated and compact to implement. The number of logic gates used should also made optimum.

### 2.2.3 GENERATION GATTING SIGNALS

The voltage from positive to negative and zero is well defined the duty cycle. From equation 2.1 , it can be seen that the ratio of output voltage to input voltage is directly proportional to the duty cycle. So if the duty cycle is increase then the output voltage will increase accordingly and vice versa.

The states that are considered for the generation of gating signals are shown in table 2.2.

TABLE-2.2
STATE CONSIDERED TO GENERATE THE GATING SIGNALS

| Q1 | Q2 | Q3 | Q4 | $\mathbf{V}_{\text {Pri }}$ |
| :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | 1 | Vin |
| 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | - Vin |
| 1 | 1 | 1 | 1 | 0 |

The time duration of voltage (positive and negative) is increased and time to zero voltage is reduced then increased the duty cycle. Similarly the time duration of (positive and negative) is decreased and time to zero voltage to be increased is decreased duty cycle.

TABLE-2.3
GENERATING REQUIRED SIGNALS FOR S1 AND S4

| Sig1 | Sig2 | Sig2' | Sig1/Sig2' ${ }^{\prime}=$ Q1=Q4 |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |

TABLE-2.4
GENERATING REQUIRED SIGNAL FOR S2 AND S3

| Sig1 | Sig2 | Sig1' | Sig2 ${ }^{\prime}$ | Sig1 $^{\prime} /$ Sig2 ${ }^{\prime}=\mathrm{Q} 2=\mathrm{Q} 3$ |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |

The two signals Sig1 and Sig2 are required switching signals. Which is controlled the four switches. Signals Q1 and Q4 are same. Similarly signals Q2 and Q3 are same. Sig1 can be generated by comparing a triangular wave with a dc voltage using an op-amp. The pulse width modulation is used in the switching mode power converter to regulate and control the output power [20].
Figure 2.2 shows the gating circuitry to generate the switching signals.


Fig. 2.2 Logic Circuit to Generate Switching Signals.
From figure 2.2, we see that triangular wave is connected to the inverting input and the constant dc voltage which is half the amplitude of the triangular wave is connected to the non-inverting input of the operational amplifier. When VDC is greater than triangular voltage V1, the op-amp makes a positive voltage. When V1 is greater than VDC, it produces zero voltage. Sig2 is generated when the reference voltage VREF which is controlled the duty cycle. If the value of VREF is increased, then the duration it is greater
than V1 will increase and the duty cycle also increased. If the VREF is decreased then the duty cycle is also decreased.

### 2.3 SINGLE INPUT DUAL OUTPUT DC-DC CONVERTER

In a single input dual output converter was presented but it requires control system constituting both duty cycle and frequency. Changing duty cycle is easily possible but changing frequency to control a load could be a complex. In addition to it, the lower load was loosely connected to the transformer primary winding. So to utilize similar control method for both of the loads, the conventional dc-dc converter to supply two separate loads is explored in this section.

### 2.3.1 CONVERTER CONFIGURATION

The full bridge single input dual output dc-dc converter configuration shown in fig 2.3


Fig 2.3 Full-bridge Single Input Dual Output Dc-dc Converter

If the turn ratios of the transformers are n 1 and n 2 and the duty cycles of the signals are D1 and D2 for two loads respectively, then the transfer functions are:

$$
\begin{equation*}
\mathrm{V}_{\text {out } 1} / \mathrm{v}_{\text {pri1 }}=\mathrm{n} 1 * \mathrm{D}_{1} \tag{2.1}
\end{equation*}
$$

And

$$
\begin{equation*}
\mathrm{V}_{\text {out } 2} / \mathrm{v}_{\text {pri2 }}=\mathrm{n} 2 * \mathrm{D}_{2} \tag{2.2}
\end{equation*}
$$

### 2.3.2 GATTING SIGNAL CIRCUITRY

As discussed in the previous, the switching signals are produced by using logic gates. Three operational amplifiers are generated the required pulses and these pulse flow through the not gates and or gates and produce four gating signals for the eight switches.

The signal Q1 is the switching signal for the switches S1 and S2, Q2 is for the switches S2 and S3, Q3 is for the switches S5 and S8 and Q4 is for the switches S6 andS7.

The single input dual output gating signal circuitry shown in fig 2.4


Fig 2.4 Logic circuit to generate switching signals

## CHAPTER-III PROPOSED DC-DC CONVERTER

### 3.1 INTRODUCTION

The proposed dc-dc converter is to reduced the number of switches comparing to the conventional single input dual output converter. As discussed in the previous chapter, single input dual output conventional dc-dc converter requires number of eight switches in total to operate two loads separately. In this thesis, the proposed dc-dc converter, to reduce the number of switches and reduced the total losses as well as each switches. Therefore, it is designed with only number of six switches and a unique switching signal is proposed to reach the optimum number of logic gates to generate the switching signals.

### 3.2 BACKGROUND AND MOTIVATION

The proposed dc-dc converter, using three switches instead of four switches in the dual output conventional dc-dc converter. Similarly, for a full-bridge dc-dc converter, if a dual output converter can be designed with reduced number of switches, it should be able to reduce cost in implementation of the regulator switches. In proposed dc-dc converter increased features, the power delivery network is required to be able to supply different voltage levels which increases cost, requires more space and consequently reduces efficiency. The dc-dc converters are broadly used in central processing unit (CPU), memory and I/O control hubs, the memory subsystem, graphics, audio, LAN etc. In PC platform, compact and high efficiency power conversion system is needed. In the field of
renewable energy, the power electronic system and hence high efficiency power conversion system is also a necessity. Due to the increased demand of power generation, the utilization of renewable energy has increased and has become more popular over the traditional fossil resources [21]. To reduce power coupling and improve system stability in distributed generation unit, implementation of virtual impedance is found useful [58]. In micro-grid system, cluster of small energy generators such as solar cells, fuel cells, wind turbine along with electrical loads exist within the main grid that includes embedded management and control system which requires power electronic converters [22].

### 3.3 DESIGN REQUIREMENTS

From the motivation to design a novel isolated dc-dc converter, the converter was designed to meet the following specifications:

1. It has the same transfer function as the conventional one so that the output is similar.
2. The output voltages can be controlled separately with load requirement.
3. Switching and conduction losses are less than the conventional one.

### 3.4 CONVERTER DESIGN AND LAYOUT

To ensure the control of the loads separately, each primary side requires four switches in the conventional one. The upper pairs of switches connect the positive input and the lower pairs ensure the connection to ground. The number of switches can be reduced by using only a pair of switch in the middle for both of the loads instead of the lower pair of switches of the upper load and upper pair of switches in the lower load. The layout of the converter is shown in figure.


Fig. 3.1. Proposed Single Input Dual Output DC-DC Converter

### 3.5 SWITCHING STATES

The next step of this thesis is the design procedure is finding the correct switching state for the converter to supply regulated voltage. By changing the switching states, the converter can have serial or parallel connection for both of the loads. For six switches with two states (on and off), the converter can have $2^{6}=64$ states. By changing the states of each switch, the voltage at the primary sides are calculated for all 64 states.

TABLE 3.1.: ALL POSSIBLE STATES

| State | S1 | S2 | S3 | S4 | S5 | S6 | Vpri1 | Vpri2 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 4 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 5 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 6 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 7 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 8 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 9 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 10 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 11 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 12 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |


| 13 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 14 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 15 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 16 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 17 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 18 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 19 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 20 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |

TABLE 3.1.: CONTINUED

| State | S1 | S2 | S3 | S4 | S5 | S6 | Vpri1 | Vpri2 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 21 | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{2 2}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{2 3}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | -Vin |
| $\mathbf{2 4}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{2 5}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{2 6}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{2 7}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{- V i n}$ | $\mathbf{0}$ |
| $\mathbf{2 8}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{- V i n}$ | $\mathbf{0}$ |
| $\mathbf{2 9}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{3 0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{3 1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{- V i n}$ | $\mathbf{- V i n}$ |
| $\mathbf{3 2}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{- V i n}$ | $\mathbf{0}$ |
| $\mathbf{3 3}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{3 4}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{3 5}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{3 6}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{3 7}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{3 8}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{V i n}$ | $\mathbf{0}$ |


| $\mathbf{3 9}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathbf{4 0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{V i n}$ | $\mathbf{0}$ |
| 41 | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{4 2}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | Vin |
| $\mathbf{4 3}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{4 4}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{4 5}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| 46 | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{V i n}$ | $\mathbf{V i n}$ |
| $\mathbf{4 7}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |

TABLE 3.1.: CONTINUED

| State | S1 | S2 | S3 | S4 | S5 | S6 | Vpri1 | Vpri2 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 48 | 1 | 0 | 1 | 1 | 1 | 1 | Vin | 0 |
| 49 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 50 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 51 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 52 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 53 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 54 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 55 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | -Vin |
| 56 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 57 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 58 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | Vin |
| 59 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 60 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 61 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 62 | 1 | 1 | 1 | 1 | 0 | 1 | Vin | 0 |
| 63 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 64 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

All 64 possible states and the respective primary side voltages are shown in table 3.1.

### 3.6 GATING SIGNALS

There are 64 possible states are used to gating switching signal consideration. All these states will be discussed in this section

### 3.6.1 SERIALLY CONNECTED LOADS OPERATE TOGETHER

When both the loads are operated at the same time then the input voltage are get divided among the primary sides voltages. The load voltage have not equal the primary voltage it is always less than the input voltage which is difficult to control.

When both loads require reduced voltage, then by controlling the duty cycle of load1 is reduced. Therefore, it provides a reduced voltage at Vpri1. But at the same time increase the voltage at Vpri2 due to the increased duty cycle of load2. Because of, from Kirchhoff's Voltage Law, for two load series connection if, decrease a voltage drop at load1 and rest of the voltage drop occurred at load 2 coming from the input. The similar difficulty will be faced if, the loads requires of increased voltage. Then the output was predicted by drawing equivalent circuits and calculation. And it possessed high risk and less efficiency for practical use as expected.

### 3.6.2 SERIALLY CONNECTED LOADS OPERATE SEPARETELY

The previous connection has a disadvantage of not getting the whole input at each of the primary sides. To avoid this problem can be to choose a gating signal in such a way that the loads do not operate at the same time. In that way one of the loads will have the whole input voltage at the primary side and the other will have zero. For example, if the first load has zero voltage at the primary side, the second one will have half of the input at the primary side and vice versa. For this state the desired states are chosen from table 3.1. Load-2 with zero primary voltage and load-1 with positive voltage can be generated from switching state $38,40,48,62$. After that Load-1 with zero primary voltage and load-2 with positive voltage can be generated from switching state 27,28 or 32 . Then load-1 with zero primary voltage and load-2 with negative voltage can be generated from the switching state 23 or 56.

TABLE 3.2.: STATES CONSIDERED TO GENERATE THE GATING SIGNALS

| Q1 | Q2 | Q3 | Q4 | Q5 | Q6 | Vpri1 | Vpri2 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | Vdc | $\mathbf{0}$ |
| $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | Vdc |
| $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | -Vdc | $\mathbf{0}$ |
| $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | -Vdc |

Any configuration can made by different states. The most suitable one to is presented in above table 3.2. The selected states to generate the gating signals are $38,23,27$ and 42 . From the table, it is seen that the switching signal Q1 and Q6 are same and Q2 and Q5 are same. And Q3 and Q4 are inverse to each other.

TABLE 3.3.: LOGIC TABLE TO GENERATE THE GATING SIGNALS

| Q4 | Sig2 | Q4 $\bigoplus$ Sig2=Q2=Q5 | !Q2=Q1=Q6 | !Q4=Q3 |
| :---: | :---: | :---: | :---: | :---: |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |

Table 3.3 presents the generation of gating signals using logic gates. Sig2 is a signal similar to Q4 but has double the frequency of Q4. These two signals can be used to generate the signal Q2 through XOR. The signal Q1 and Q3 can be generated by simply using not in the signals Q2 and Q4 respectively. As mentioned before, Q5 is the same signal as Q2 and Q6 is the same signal as Q1.


Fig. 3.2. Primary Side Voltages of the Loads for Series Connection
The voltages of the primary sides of the transformer look like above figure. In this case, the problem faced about having the source voltage at the primary side in the previous design was eliminated. As the loads do not operate at the same time, the input voltage is present with the whole magnitude in the primary side voltage. If the generated input voltage is lesser than the required input voltage, then the output voltage at the loads will be less too. In that case, to reach the required voltage level, the duty cycle needs to be boosted.


Fig. 3.3. Primary Side Voltages with Increased Duty Cycle for Load-1

In figure 3.3 shows that the primary sides for the loads if the duty cycle for load- 1 is increased. From the figure, it is observed that, when the duty cycle for load-1 increases, to ensure the voltage level Vdc at the primary side for the load-1, the duty cycle for load-2 has to be decreased. Hence the source voltage will get divided among the loads. The problem of not having Vdc as primary side voltage like the previous design will still remain. Also depending on the load condition, the voltage level will fluctuate and hence will be difficult to control. Similarly, if the duty cycle for load-2 in needed to be increased, then duty cycle for load-1 must have to decrease to ensure consistent voltage at primary sides. So this arrangement lead to either compensate one of the loads for the other or have different unwanted and unpredictable voltage levels at the primary sides. It also makes the duty cycles dependent on each other as the load that is being compensated is forced to a smaller duty cycle to ensure larger duty cycle to the other. Similar situations are applicable when lower voltage is required. This configuration will work great for the situations where both of the loads are complete opposite in terms of voltage requirements and are somewhat dependent on each other in increasing and decreasing load requirements. So a decision can be made from this design that although the loads can operate with different duty cycle and hence can generate different levels of output voltage, the problem with independent control of the loads still prevalent during this connection.

### 3.6.3 PARALLEL CONNECTION OF THE LOAD

From another combination from table 3.1, a parallel connection of the loads can be made. For parallel connection, the positive node of the source voltage is connected to the same upper or lower node of both of the loads. Similarly the ground is connected to the same upper or lower node of both of the loads. During this configuration, both loads can operate at the same time with different duty cycles. The duty cycle of load-1 and load-2 can be
control separately. This connection solves the problem of dependency on each load. Therefore, for this design, this connection was chosen.

### 3.7 SELECTION OF GATING SIGNAL FOR THE PROPOSED CONVERTER

The parallel connection was discussed in the previous section, for this design. The states should be chosen such that the switches operate such that the loads get connected in parallel rather than in serial. From table 3.1, during state 46 both of the loads have positive source voltage at primary sides and during state 31 , they have negative source voltage at the primary side. So, these two states should be taken into consideration as they must be ensures parallel connection of the loads.

## TABLE 3.4.: DESIRED SWITCHING STATES

| S1 | S2 | S3 | S4 | S5 | S6 | Vpri1 | Vpri2 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | Vdc | Vdc |
| $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | -Vdc | -Vdc |
| $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |

Table 3.4 shows the desired switching states for generating the gating signals. Other two states, where the loads have zero voltage at primary sides, are chosen such that the logic circuitry to generate the switching signals is convenient. Switching signal Q1 and Q2 are normally the inverse to each other. If the signal Q1 can be generate then passing Q1 through a NOT gate will generate the signal Q2.

TABLE 3.5.:
GENERATION OF THE SWITCHING SIGNALS FOR THE SWITCHES Q1 AND Q2

| Sig1 | Sig2' | $\left(\right.$ Sig1 $\oplus$ 'Sig2') ${ }^{\prime} \mathbf{1 1 ~}^{\prime}$ | $\mathrm{Q}^{\prime}=\mathrm{Q}^{\prime}$ |
| :---: | :---: | :---: | :---: |
| 1 | 0 | 1 | 0 |


| 1 | 1 | 0 | 1 |
| :--- | :--- | :--- | :--- |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |

The $\operatorname{Sig} 1(\mathrm{Op}-\mathrm{Amp} 1)$ and $\operatorname{Sig} 2(\mathrm{Op}-\mathrm{Amp} 2)$ are used to generate the other signals similar to the one in serial connection. Sig1 and sig2 are generated by comparing a triangular wave with a reference dc voltage.

Sig2' is the inverse of Sig2. Signal Q1 can be generated by passing the signals Sig1 and Sig2' through an XOR gate. Generation of Q1 and Q2 are shown in table 3.5.
The Sig2 is same the signal Q3 in table 3.4, this signals contribute to the duty cycle for primary side voltages. So they are needed to be controlled separately.

TABLE 3.6.
GENERATION OF THE SWITCHING SIGNALS FOR THE SWITCH Q3

| Q2 | Sig2 | (Q2\|Sig2)Sig3 | (Sig2\&Sig3)Q3 |
| :---: | :---: | :---: | :---: |
| $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ |
| $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ |
| $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ |
| $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |

Table 3.6 shows how the signal Q3 can be generated from Sig2 and Q2. First these signals are passed through an OR gate then an intermediate signal Sig3 is generated. From Sig2 and Sig3, signal Q3 is found.

The above table is used when the duty cycle is the same but the control of the duty cycle of the second load, Sig2'2 is used too to generate the signal. Finally produced Q3 signal is as follows

TABLE 3.7.:
GENERATION OF THE SWITCHING SIGNALS FOR THE SWITCH Q3

| $\mathbf{Q 2}$ | Sig2'2 | (Sig2'2\|Q2)Sig3 | (Sig2\&Sig3)Q3 |
| :---: | :---: | :---: | :---: |
| $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ |
| $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ |


| $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ |
| :--- | :--- | :--- | :--- |
| $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ |

Table 3.7 shows the ways to generate the signal for switch Q3 by using both the controlling signal for load-1 and load-2.
Also signal Q4 looks same as signal Q3 from the table, If the signal Q4 and Q3 are middle, So they are controlling for both the upper load and lower load. So their operation time should be different depending of load-1 and load-2. signals Sig2 that controls the duty cycle for load-1 and Sig2'2(Op-Amp 3) that controls the duty cycle for load-2 need while generating the switching signal for Q 4 .

TABLE 3.8.
GENERATION OF THE SWITCHING SIGNALS FOR THE SWITCH Q4

| Q2 | Sig2'2 | (Q2(AND)Sig2'2)Sig4 |
| :---: | :---: | :---: |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |
| 0 | 0 | 0 |


| Q1 | (Sig4(OR)Q1)Sig5 | (Sig5(AND)Sig2)Q4 |
| :---: | :---: | :---: |
| 1 | 1 | 1 |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

Table 3.8 shows the generation logic for Q4. First an intermediate signal Sig4 is formed from Q2 and Sig2'2. Then from this Sig4 and Q1, another intermediate signal Sig5 is formed using OR gate. Then again from this Sig5 and Sig2, the signal Q4 is finally generated through an AND gate.

### 3.8 OPERATING PRINCIPLE

In this section operating principle are described in four required states

STATE 1 The generation of voltage Vpri1, when the switches Q1, Q4 and Q6 have to be on then conducting load-1. When switch Q 3 also is also on then both loads are conducting Only the switch Q3 during this time ensures connection of load-2. During this time load 2 has positive voltage on the primary and secondary sides. This situation is shown in figure 3.5. The parallel connection of the loads ensures positive voltage at both of the primary sides. As can be seen from the figure that when both of the loads are operating, switch S1 and S3 are connected to the same node +Vin and the switches S4 and S6 are connected to the same ground node.


Fig. 3.4. Equivalent Circuit for the First State

STATE 2 In this state only switches S 2 and S 5 are conducting. As no path is fulfilled, no current flows and the source get disconnected from the load and get zero voltage. this section, it needs to be ensured that the switches S3 and S4 are open, so that they couldn't create any path for current flow and result is zero voltage is produced.


STATE 3 Fig. 3.5. Equivalent Circuit for the Second State
STATE 3


Fig. 3.6. Equivalent Circuit for the Third State

When switches S2, S3 and S5 are on then controls load1. But when switch Q4 also on it control the load2. Figure 3.6 shows the equivalent circuit and the direction of current flow during this state. During this state, the switches S3 and S5 are connected to the ground when operate and switches $S 2, S 4$ and $S 6$ are connected to the same node as +Vin when operate. So the voltages at primary sides of the loads are

$$
0-(+ \text { Vin })=- \text { Vin }
$$

Thus both of loads have negative voltage at primary sides.

STATE 4 This state is similar to state-2. Here Switches S1 and S6 are closed without making any circuit path. All other switches have to stay open so no current making path is make for the load. Figure 3.7 shows the equivalent circuit for this state.


Fig. 3.8. Equivalent Circuit for the Fourth State

### 3.9 SWITCHING SIGNAL CIRCUITRY

The generating of switching signals, here the both triangular wave is compared with the reference voltage. For output1, the duty cycle can vary up to the maximum, which is 1 . But output 2 can reach the duty cycle equal to D 1 . The reference voltage can vary according to the output voltage considering the range. From figure 3.9 the Sig1 is used for switch S1 and S6, the Sig2 used for switch S2 and S5 and Sig3 and Sig4 are used for switch S3 and S4 respectively.


Fig. 3.9. Circuitry to Generate Gating Signals

## CHAPTER- IV

## RESULTS AND SIMULATION

### 4.1 INTRODUCTION

The theoretically analysis is needed to ensure that the design works for real-life situations. The previous chapter was drawn the converter design and simulated to the design. In this chapter, the results obtained from the simulations are discussed and verified. The Switching loss and conduction losses are obtained and calculated for the conventional and proposed converters. The comparative analyses are also presented in this chapter. Electronic circuit will be simulated by the software PSIM [23].

### 4.2 CIRCUIT DIAGRAM TO SIMULATE PROPOSED DC-DC CONVERTER

While implementing the design at first, the MOSFETs were used in the schematic. From the menu bar in PSIM, "Elements" was clicked. After that from the menu bar drop down menu, Power ~ Switches~ MOSFET was selected to six MOSFETs and placed in two columns as the switches of the converter. The source in a dc voltage is drawn from the Elements $\sim$ Sources $\sim$ Voltage $\sim$ DC was selected as the input dc voltage. The values of the components are taken by double clicking of the elements and entering the value of magnitude. The other components are selected from the Elements $\sim$ Power module. In the module, the resistors, capacitors and inductors are placed from the "RLC Branches". There is a subsection named" Transformers" in the "Power" module. The transformers are selected from that subsection. Then the diodes are placed from the "Switches" subsection. After the placement of the elements in their suitable positions, they are connected through wires. The ground was connected at the bottom of the diagram for proper current flow
through the circuit. The gating signals connection in the diagrams by wires can makes the complicated and cumbersome. Also it contains various logic gates and there are chances of wrong connections and misplaced nodes. For that reason, the gating signal circuitry was placed separately and the labels were used to provides the signal inputs in the switches. The switches cannot be connected to the labels through wires. An additional element is required among the switches and the signal. Elements~ Other~ Switch Controllers ~OnOff Controller was selected and placed among the switches and their corresponding signal labels.


Fig. 4.1. Diagram in PSIM to Simulate the Designed Converter

In the figure of 4.1 the diagram is drawn on PSIM. At the 1st stage of the simulation, MOSFETs are used as switches for simplicity. After successful evaluation of the design, practical switches are employed instead of the ideal ones. The MOSFET switches are an active switch with an anti-parallel diode. MOSFET will be turned on if the gating signal is a logic high and the switch is positively biased (drain-source voltage is positive).After that the gating signal will be low or the current drops to zero and consequently it turns off. Now
for the gating circuit, the logic gates are selected from Elements $\sim$ Control $\sim$ Logic Elements. Then the Op-Amps are found in the "Other" subsection of the "Power" module.


Fig. 4.2 Gating Circuitry to Generate the Switching Signals
Figure 4.2 generate the switching signals in PSIM. There are four signals which was generated here as signals Sig1 was used as the switching signals for the sixth and fifth switches and sig2 used for the first and second switches. The labels are placed in the parts where the desired signals are generated. Connecting these labels as the gating signals to the switches, the "On-off Controllers" are required. On-off switch controller works as the connecting between the control gating signals and the power switches. The switches are controlled by the gating signal which are the input logic signal generated from the control circuit is passed to the power circuit [24]. The "On-Off Controllers" are placed between the signal labels and the power switches.

### 4.3 RESULTS FROM SIMULATION

After the circuits are completed then the menu bar "Simulation" is clicked and from the drop down menu and "Simulation Control" is selected. After that the cursor changes into a clock symbol. This clock is placed at a side on the schematic. Then change the properties of the time step, total time etc.

TABLE-4.1
PARAMETERS OF SIMULATION CONTROLS

| Parameters | Value |
| :---: | :---: |
| Time step | 4E-006 |
| Total time | 1.01 |
| Print time | 1.004 |
| Print step | 1 |

The parameters of the "Simulation Control" are shown in table 4.1. Then the simulation is run by selecting "Run Simulation" from "Simulation" menu. After the simulation is completed, "Run SIMVIEW" is selected. Then by selecting the waveforms of the previously placed probes, the waveforms are displayed. The required switching signals found from the simulation are shown in figure 4.3.





Fig. 4.3 Four Switching Signals Generated to Control the Voltage at Primary Side.

In load-1 and load-2 are separately controlled by the different duty during this simulation. So the duty cycle for load-1 (the upper load) is 1 and the duty cycle for load-2 (the lower load) is 0.5 .In this simulation, the input voltage is set as 30 volts. The turns ratios of the transformers are 1:2 for both of the loads. The output voltages of load-1 and load-2 are found from this simulation are shown in figure 4.4


Fig 4.4 Output Voltages of Load-1 and Load-2

### 4.4 CALCULATIONS

From the transfer function of the converter, the output voltages can be calculated. Equation (2.2) in chapter 2 of this thesis gives the transfer function of load-1 of the converter and equation (2.3) gives the transfer function of load-2 of the converter.

From figure 4.5, the output voltage for load-1 is approximately 60 volts and the output voltage for load-2 is approximately 32 volts

For load-1, the output voltage calculated for this case is,

$$
\begin{aligned}
\text { Vout } 1 & =\mathrm{n} 1 * \mathrm{D} 1 * \text { Vpri1 } \\
& =2 * 1 * 30 \\
\text { Vout } 1 & =60 \mathrm{~V}
\end{aligned}
$$

For load-2, the output voltage calculated for this case is,

$$
\begin{aligned}
\text { Vout } 2 & =\mathrm{n} 1 * \mathrm{D} 2 * \text { Vpri } 2 \\
& =2 * 0.5 * 30
\end{aligned}
$$

Therefore, Vout $2=30 \mathrm{~V}$
Both the outputs are matches the simulated output results in figure 4.4.

### 4.5 COMPARISON WITH THE CONVENTIONAL CONVERTER

### 4.5.1 GENERATION OF OUTPUT VOLTAGE

In the real field of application of dc-dc converter, the input voltage can fluctuate. Particularly in the field of applications of renewable energy, the dependency on the environment, weather and location is huge and so that the generation of power can vary a lot [74]. In that case, the voltage needs to be regulated. As for example, if the input voltage reduces, then the generation of output voltage will be less to. So the duty cycle needs to be increased to meet the power requirement. With a closed loop feedback control system it can be easily done. By changing the input voltage and Reference voltage output voltage was generated for similar condition in conventional and the designed converter.
The result is below in table 4.2

TABLE-4.2
OUTPUT VOLTAGE OF CONVENTIONAL AND PROPOSED CONVERTER WITH CHANGING INPUT VOLTAGE AND REFERENCE VOLTAGE

| Vin | VREF1 | VREF2 | Vout1 <br> (conv.) | Vout2 <br> (Conv.) | Vout1 <br> (proposed) | Vout2 <br> (proposed) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 20 | 12 | 8 | 16.751 | 11.978 | 16.757 | 11.969 |
| 30 | 12 | 8 | 25.17 | 17.965 | 25.135 | 17.96 |
| 30 | 14 | 14 | 29.895 | 29.895 | 29.881 | 29.881 |
| 20 | 14 | 14 | 19.96 | 19.96 | 19.92 | 19.92 |

The table 4.2 exhibit the proposed converter voltage is similar voltages as the conventional one with input voltages. So the proposed dc-dc converter is able to meet the requirement just like the conventional one but with increased efficiency to operate with reduced number of switches.

### 4.5.2 POWER LOSS

In this subsection, we calculated the power loss of conventional and proposed dc-dc converter and comparison between them. There are two types of power losses occurred in every MOSFET switches, Firstly, the conduction losses and Secondly, the switching losses.

The transistor conduction loss is calculated as:

$$
\begin{equation*}
\text { Transistor Conduction Losses }=\mathrm{I}_{\mathrm{D}}^{2} * \mathrm{R}_{\mathrm{DS}(\mathrm{ON})} \tag{4.1}
\end{equation*}
$$

Where, $\mathrm{I}_{\mathrm{D}}$ the drain current, and $\mathrm{R}_{\mathrm{DS}}(\mathrm{on})$ is the static on-resistance.

When the transistor is conducting periodically with an on duty cycle of D , the conduction losses are calculated as:


Fig. 4.5 Waveform of currents of conventional converters for various MOSFET.

Figure 4.5 contains the current waveforms in all of the switches in the conventional configuration. Using equation (4.2) and taking value of current from the current waveform of figure (4.5) we get the conduction losses of eight switches. The loss of four switches (S1,S4,S5,S8) is approximately 0.7168 watts each and the loss of other switches (S2,S3,S6,S7) is approximately 0.1792 each. The total losses of eight switches are 3.584 watts. Therefore, the average losses of each switches is approximately 0.4475 watts.


Figure 4.6 contains the current waveforms in all of the switches in the conventional configuration. Using equation (4.2) and taking value of current from the current waveform of figure (4.5) we get the conduction losses of eight switches. The loss of two switches (S1, S6) is approximately 0.564 watts each and the loss of another two switches (S2, S5) is approximately 0.141148 each and the rest of the switches ( $\mathrm{S} 3, \mathrm{~S} 4$ ) is approximately 0.181 watts. The total losses of six switches are 1.77 watts. Therefore, the average losses of each switches is approximately 0.295 watts.

The proposed configuration conduction loss has two times less conduction loss than the conventional one. This loss is much reduced because of the selection of proper switching signal that has reduced the conduction losses in the middle two switches greatly.


Fig. 4.7 Comparison between the Conduction Losses of the Conventional and Proposed Configuration.

The switching losses of the MOSFETs are the turn on and turn-on losses. The transistor turn-on loss is calculated as:

Transistor turn-on Losses $=$ Eon $*$ fsw

Where, Eon is the transistor turn-on energy losses and f is the frequency as defined in the input parameter "Frequency".

Where, $\mathrm{EON}=\mathrm{V}_{\mathrm{DD}} * \mathrm{I}_{\mathrm{D}(\mathrm{ON})} * \frac{\text { tri+tfv }}{2}$
Where, $\mathrm{t}_{\mathrm{ri}}$ is the current rise time from zero to switch ON state and $\mathrm{t}_{\mathrm{fv}}$ is the voltage fall time from maximum to zero.

The transistor turn-off loss is calculated as:
Transistor turn-off Losses $=$ EofF $* \mathrm{f}_{\mathrm{s}}$
Where, Eoff is the transistor turn-off energy losses.

$$
\text { Therefore, EOFF }=\mathrm{V}_{\mathrm{DD}} * \mathrm{I}_{\mathrm{D}(\mathrm{ON})} * \frac{\text { tfi}+ \text { trv }}{2} \ldots \ldots \ldots \ldots . \text { (4.6) }
$$

Where, $\mathrm{t}_{\mathrm{rv}}$ is the voltage rise time from zero to switch OFF state and $\mathrm{t}_{\mathrm{fi}}$ is the current fall time from maximum to zero. The energy losses is calculated by using the rise times and the fall times of the voltage and current waveforms based on the information of the MOSFET gate current, input/output/reverse transfer capacitances and gate charges.


Fig. 4.8 waveforms of currents of switching losses of the Switches in conventional Design.

Figure 4.5 contains the current waveforms in all of the switches in the conventional configuration for switching losses calculation. Using equation (4.3, 4.4, 4.5 and 4.5) and
taking value of current from the current waveform of figure (4.8) we get the switching losses of eight switches. Just like the conduction losses, the switching losses are almost same for all eight switches in this configuration which is approximately 0.104 Watts each. The total losses of eight switches are 0.834 watts.





Fig. 4.9 waveforms of currents of switching losses of the Switches in proposed design.

Figure 4.9 contains the current waveforms of the switching losses in the proposed design. In this case, the switching losses for the first two and the bottom two switches are almost same (approximately 0.09696 Watts each). The middle two switches have a slightly higher switching loss (approximately 0.0485 Watts) than the other four switches. Similarly to the conduction losses, the higher switching loss in the proposed design is smaller than the lowest conduction loss among the switches. Hence, the total switching loss in the proposed converter is much less which is approximately equals 0.48484 Watts. The comparison among the total switching losses between the conventional and the proposed converter is
shown using a pie chart in figure 4.10. The total switching loss in the proposed converter is about 1.7 times less than the total switching loss in the conventional configuration.


Fig.4.10 Comparison between the Switching Losses of the Conventional and Proposed Configuration.

The total losses in the switches are calculated by summation of conduction loss and switching loss. A measuring device (an ammeter in this case) is connected at the node that joins all of the transmission paths from the four nodes that depict the conduction and switching losses of the transistors and diodes. The total loss for the conventional configuration is almost 4.418 Watts and the total loss for the conventional configuration is
almost 2.25484 Watts. Total losses in conventional and proposed converter are compared in figure 4.8 by using a pie chart. For similar loads, transformer ratio, input conditions and duty cycles, the proposed converter has around $49 \%$ less switching and conduction loss than the conventional one.


Fig.4.11 Comparison between the Total Losses of the Conventional and Proposed Configuration.

## CHAPTER-V

## CONCLUSION AND FUTURE RESEARCH

### 5.1 CONCLUSION

The dc-dc converter is able to transforming the input voltage to any desired voltage. In according to our requirement if needed more voltage than used step up transformer used to voltage up and for less voltage achieved by step down transformer. The proposed converter is capable to the similar work like conventional converter. The result of designed converter shown in previous chapter there only six switches generate the same output like at eight switches. Therefore, the total losses of proposed converter are much lower than the conventional converter. Also the PWM circuitry has almost same number of logic gates as the conventional one. So the designed converter has better efficiency from several points.

### 5.2 SUGGESTED IMPROVEMENTS

The whole system could be implementation of a wireless control system. If a wireless feedback system can be developed that is capable of sending the pulse width modulated signal to the converter with desired duty cycle, then the converter can be controlled from a remote position according to user requirements. Real-time regulation can be possible by implementing feedback system along with this proposed strategy.

## References

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