IMPACT IONIZATION DEPENDENCE OF HOLE TRAPPING PHENOMENA IN HEMTS

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Abstract: *Impact ionization effects on hole trapping phenomena In high electron mobility transistor (HEMT) is investigated. For the purpose, measurement and a trap model simulation was done for two test devices. Measured and simulated hole trapping time constant and hole trap voltage for the two test devices are calculated and their dependence on drain bias are explored to correlate the effect of impact ionization on hole trapping phenomena. The model usability for device with different impact ionization behaviour is explored.*
Keywords: *HEMT, Trap charge, impact ionization*

I. Introduction

Impact ionization effects hole trapping phenomena. Hole trapping effects incorporate voltage due to charge in traps and time required to store and decay of the charge. The charge in traps give rise to a voltage named trap voltage, and the time needed to store or decay charge in traps is known as trapping time constant. To investigate impact ionization dependence of hole trapping, measurements are done with two different HEMTs. HEMTs are chosen as they are extensively used in RF applications for their suitability in high frequency application. It is observed that due to impact ionization, not only does the trapping time constant decreases dramatically at high drain voltage, but negative charge due to trapping (trap voltage) also decreases. A trap model was developed where charge in hole trap was modelled as a nonlinear voltage, while the time constant by a nonlinear resistor capacitor circuit [1]. The model's usability for weak and strong impact ionization device is also tested in this work.

2. Impact Ionization

Impact ionization is a carrier multiplying phenomena that occurs in devices at high electric fields. At high electric field, channel electrons gain energy larger than the band gap of the semiconductor, high energetic carriers collide with the crystal lattice. A high energy electron in the conduction band scatters from an electron in the valence band. The second electron is raised to the conduction band, a new electron is created in conduction band and a hole is created in valence band. This carrier multiplication results in dramatic increase in current.

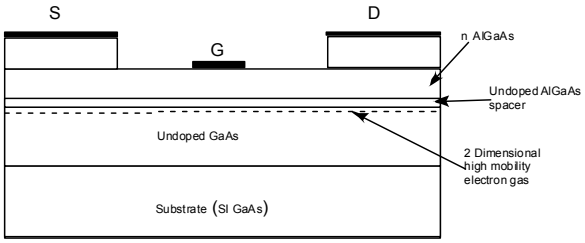

Fig. 1 A typical HEMT structure.

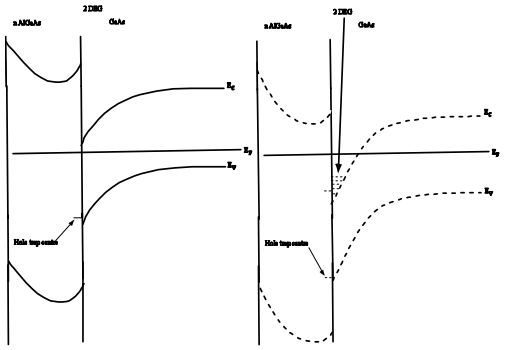

Fig. 2 Energy band diagram for the HEMT structure, for turn off condition (left), and turn on condition (on) of the device.

3. HEMT Structure, Band Diagram and Hole Trapping Mechanism

The structure of a typical AlGaAs/GaAs HEMT is seen in Fig 1. The structure is a depletion device or normally on device, i.e., a conducting channel is formed when zero bias

is applied at the gate. The device can be turned off by applying negative voltage at the gate. Negative voltage drives electrons away from the channel and thus depletes the channel. An energy band diagram for the device is shown in Fig. 2. The left diagram represents band diagram for turn-off condition when the channel is pinched off by the application of a negative voltage, while, the right represents the device turn-on condition when conducting channel forms with zero volts applied at the gate.

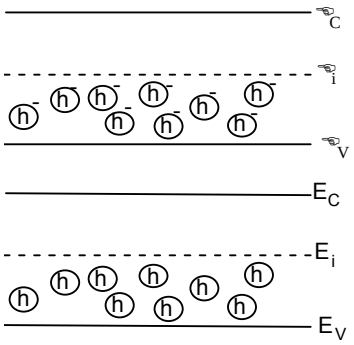

Fig. 3 Schematic diagram of hole traps at turn-off (top) and turn-on (bottom) condition.

Traps act as either electron or hole traps according to their position in the energy band gap. Trap centres lying below the mid band gap level usually act as hole traps. In Fig. 2, one hole trap state has been shown for ease of explanation. Figure 3 shows a schematic diagram of charge in electron and hole traps during turn-off and turn-on condition. When the device is turned off, i.e., a negative gate bias is applied, the channel gets pinched off. Hole trap states, being below Fermi level, capture electrons and become negatively charged [2]. If the drain bias before turn-off is high enough to start impact ionization in the channel, then more holes are available in the channel that result in greater number of hole traps filled with holes at the time of turn-off. Thus at high drain bias condition (when impact ionization begins), less hole traps capture electrons resulting in smaller amount of negative charge. When, gate is pulsed to zero volts, hole traps capture holes from the channel valence band and release the negative charge associated with them. This hole capturing is not instantaneous. The time constant related to hole capture depends on energetic position of trap centre and number of holes available for capture. So the negative charge in the hole traps takes sometime before decaying, and thus causes delay. This negative charge stored in hole traps during turnoff give rise to a voltage that can be called trap voltage. The delay in decaying of the trap voltage leads to delay in drain current rise to its steady state value, which is gate lag as seen in Fig 4. For any drain bias the lag time is equal to hole trapping time constant. Gate lag measurements are done using an arbitrary pulsed semiconductor parameter analyzer (APSPA) [3]. The initial slight decrease of drain current is caused by electron capture mechanism. Electron traps are positively charged when empty and this charge decays by capturing electrons during turn-on.

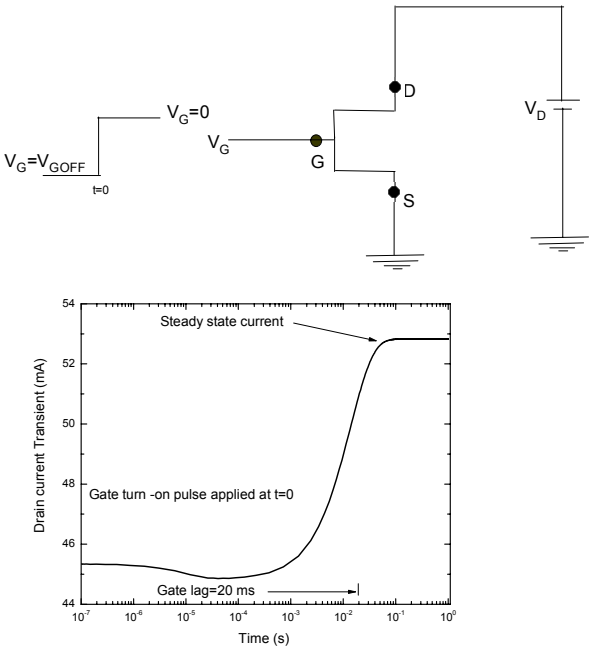

Fig. 4 A typical drain current transient after turn on pulse at the gate of an off device.

Electron trapping has been analyzed and modelled elsewhere [5]. It has been found both in our measurements and work done previously [2], [4] that in these devices concentration of surface electron traps are much less than that of hole traps.

4. Trapping Time Constant

Of the two test devices, one shows strong impact ionization, while, the other shows weak impact ionization. Both devices have the same breakdown voltage. Measured and

modelled hole trapping time constant of two test devices are seen in Fig. 5.

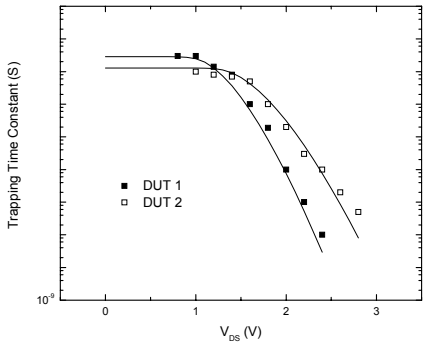

Fig. 5 Comparison of trapping time constant of the two test devices. Calculated from gate lag measurement of drain current transients of gate lag measurements at V_{GOFF} = -1.4 V.

DUT 1 has faster hole trapping time constant than that of DUT 2. Especially, trapping time constant falls rapidly at higher drain voltages in DUT 1. At high drain voltage because of onset of impact ionization, the number of holes in the channel increases. This presence of greater number of holes in the channel results in quicker trapping of hole traps, that is, shorter time constant [4], [6], [7], [8]. Figure 5 shows that at high drain voltages the decrease of trapping time constant with drain voltage in DUT 1 is faster than that of DUT 2, which indicates stronger impact ionization in DUT 1 than DUT 2. Gate current versus drain voltage measurement for the two test devices are seen in Fig. 6.

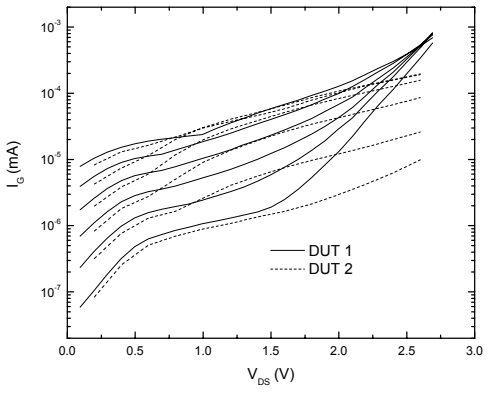

Fig. 6 Comparison of gate current versus drain voltage of two test devices, V_{GS} from 0 V to -0.5 V at a step of -0.1 V.

It is seen that for DUT 1, gate current starts to rise abruptly with increasing drain biases. This is due to impact ionization generated holes collected at the gate that cause sharp rise in gate current at higher drain voltages [6].

5. Trap Voltage

In Fig 4, the drain current after the turn-on pulse is Id_initial and drain current after 1 second is I_{d_final}. Thus Id_initial is the current when traps are negatively charged, while I_{d_final} is drain current after hole capture is complete that is the negative charge in the traps have decayed [2]. The difference between these two current ($I_{D\square}$ = I_{D_final} − $I_{D\_initial}$) is associated with hole trap potential $V_{HoleT\ rap}$. With the assumption that hole trapping has a time constant greater than 100ns, drain characteristics with 100ns pulse gives drain current without trapping for any gate/drain voltage. The $V_{HoleT\ rap}$ at any VDS was calculated from the gate voltage corresponding to ID_ in this characteristics. Measured and modelled trap voltage for the two test devices are seen in Fig. 7.

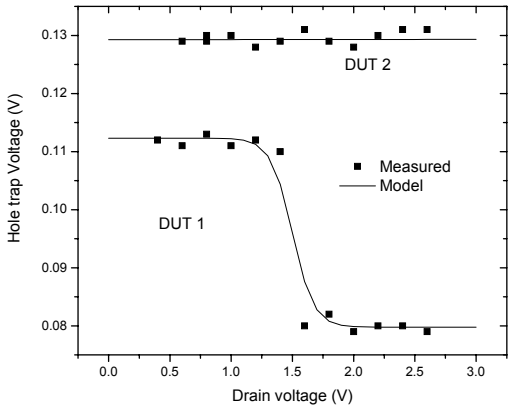

Fig. 7 Comparison of trap voltage of the two test devices, measured and modelled.

For DUT 1, hole trap voltage decreases with the increase of drain voltage; while for DUT 2, trap voltage is nearly independent of drain voltage. The decrease in trap voltage is due to presence of greater amount of holes in the channel at higher drain voltages. With the onset of impact ionization, the number of holes increase in the channel at high drain bias, so when the device is turned off, less number of hole traps are available for electron capture and getting negatively charged [2]. Thus the trap voltage is less

when impact ionization takes place. The trap model can correctly model the hole trap voltage for both strong and weak impact ionization type device. In DUT 1, the decrease of trap voltage and sharp decrease of trapping time constant both occur at the same drain bias (approximately at VDS = 1.4V), where strong impact ionization starts. To investigate further, drain characteristics for both the devices in the presence and in the absence of trapping needs to be examined. Trapping is associated with finite time constant. At gate and drain bias of zero voltage no trapping is present. If the device is pulsed to a certain V_{GS} and V_{DS} from zero gate and drain voltage, and drain current is measured in a short time, then the drain current corresponds to that without the effect of trapping at that VGS and VDS. This can be achieved by the application of 100ns gate and drain pulse at a bias condition of VGS = 0 and VDS = 0 and measuring the drain current. Similarly, as trapping is associated with finite time, if the drain current is measured after a significant time of application of gate and drain pulses, it will incorporate the effects of trapping. So to measure drain current with the effects of trapping, a 1s pulse is applied (considering trapping time constants less than 1s) at the gate and drain at a bias condition of VGS = 0 and VDS = 0 and drain current is measured.

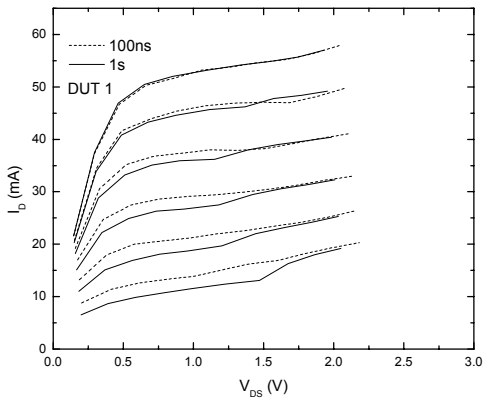

Fig. 8 Drain characteristics with 100ns and 1s pulse for DUT 1 (device having stronger impact ionization) V_{GS}=0 to -0.5 V at a step of -0.1 V.

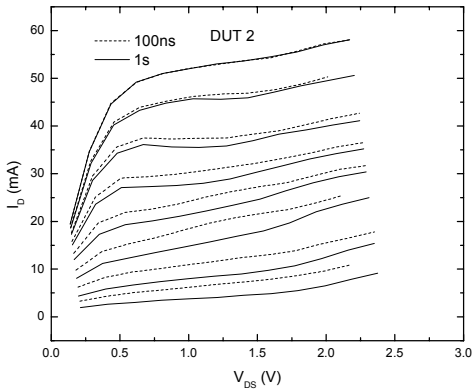

Fig. 9 Drain characteristics with 100ns and 1s pulse for DUT 1 (device having stronger impact ionization) V_{GS}=0 to -0.5 V at a step of -0.1 V.

Figs 8 and 9 show the drain characteristics with 100ns pulse and 1s pulse for DUT 1 and DUT 2, respectively. The 100ns pulse characteristics show the drain current without trapping effects while, the 1s characteristics show the drain current including trapping effects. The difference between these two drain current corresponds to the current due to hole trapping voltage of Fig. 7. In Fig. 8, it is seen that for DUT 1, the difference between drain current characteristics for 100ns pulse (without trapping) and 1s pulse (with trapping) decrease at higher drain bias. The 1s characteristics show impact ionization caused sudden sharp rise in drain current at high drain voltages and the difference between 100ns (without trap) and 1s (with trap) characteristics nearly diminishes. Lesser difference in 100ns (without trapping) and 1s pulse (with trapping) characteristics at high drain biases is due to smaller amount of hole trap voltage as seen in Fig. 7. However, close observation in Fig. 9 for DUT 2 shows that, in 1s characteristics (with trapping), for high gate biases (VGS > −0.4), drain current drops slightly at intermediate drain voltages and then increases again at higher drain voltages. This is due to the presence of oscillation rather than strong impact ionization. However, for low gate bias voltages (VGS < −0.4), there is an increase in drain current in 1s characteristics at higher drain biases, but it is not as prominent as that in DUT 1. Though the difference between 100ns and 1s characteristics decrease, this decrease is less than that of Fig. 8. When there is an exponential rise of gate current with increasing drain bias, the hole trap

voltage decreases (strong impact ionization case), while, if the gate current rise with increasing drain bias is not significant, the hole trap voltage remains nearly constant with increasing drain bias (weak impact ionization case). It is observed that due to impact ionization, not only does the trapping time constant decreases dramatically at high drain voltage, but negative charge due to trapping, hence trap voltage, also decreases. Strong impact ionization condition leads to the presence of ore channel holes, which in turn, results in less negative charge in hole traps at negative gate bias condition, leading to smaller hole trap voltage.

6. Conclusion

In this paper an investigation of impact ionization effects on hole trapping is made and usability of a previously developed trap model's for devices showing strong or weak impact ionization has been tested. Extensive gate lag measurements and model simulations have been done for both devices; the results with DUT 1 can be found at [1], [5] and DUT 2 will be published elsewhere. Of the two test devices, one (DUT 1) showed strong impact ionization, while the other (DUT 2) showed weak impact ionization in the normal operating voltage. Both devices had same breakdown voltage. It has been found that in case of strong impact ionization, hole trapping effect reduces at higher drain voltages, which is associated with the presence of greater amount of holes in the channel. Onset of impact ionization results in decrease of hole trap voltage and trapping time constant thus in effect reduces hole trapping phenomena.

7. References

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